UNIT IV : BOOLEAN ALGEBRA, ARITHMETIC AND COMBINATIONAL LOGIC CIRCUITS

Basic laws of Boolean algebra - De Morgan's theorem - Verification of Boolean expression using Boolean laws - Half-adder - Full adder - Half-Subtractor- Full subtractor (using basic gates) – Encoder - Decimal to BCD encoder- Decoder- BCD to decimal decoder.

UNIT V : SEMICONDUCTOR MEMORIES

Introduction – ROM using diodes and transistors – ROM in terms of digital circuits – Building memory of larger capacity – PROM – EPROM – EEPROM – ROM as a unit in microcomputers – RAM – Static RAM – Flip – Flop as a RAM cell – Memory expansion _ Memory Parameters.

UNIT - I
CURRENT ELECTRICITY

a. Ohm's Law

The current flow through a conductor depends upon the potential difference applied.

Ohm's law states that when the temperature .emains constant, the potential difference between the ends of the conductor is directly proportional to the current flowing through the conductor.

Potential difference $\propto$ current

$$\text{or} \qquad V \propto I \quad \text{or} \quad \frac{V}{I} \text{ constant } R$$

$$\therefore V = IR$$

Here R is a constant called the resistance of the conductor. It is measured in the unit of ohm. When the p.d is measured in volt and the current in ampere, then,

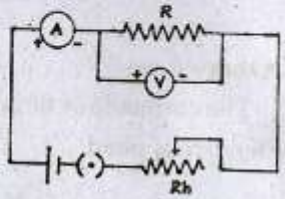
$$1 \text{ ohm} = \frac{1 \text{ volt}}{1 \text{ ampere}}$$

From this we can define the unit of resistance. The ohm is defined as the resistance of a conductor in which a potential difference of 1 volt is developed when current of I ampere flows through it or simply ohm is the ratio between volt and ampere.

Verification of ohm's law:

Ohm's law can be verified using a simple circuit shown in figure. The current through the circuit can be varied with the help of a

rheostat connected in series with the battery. The current can be measured using the ammeter. The p.d across the resistance R can be measured using the voltmeter V.



Using the rheostat, the current through the circuit is kept at a particular value I. Now the voltmeter reading is noted. Let it be V. Then V/I is calculated.

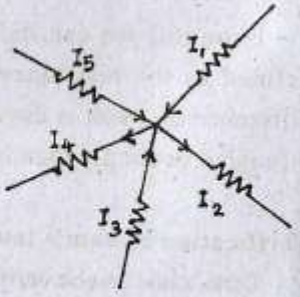
Similarly by changing the current, for each current the p.d across the resistance is noted. For each current V/I is calculated. It is found to be a constant. This verifies the Ohm's law.

b. Kirchhoff's Law

In a simple circuits consisting of battery and resistance in series or parallel, we can apply Ohm's law to calculate the current and the potential differences. If the circuit is complicated we cannot use Ohm's law. For such a circuits Kirchhoff's law can be used.

(i) Kirchhoff's First Law: In any network of conductors in an electrical circuit, the algebraic sum of currents meeting at any point is zero or sum of the currents flowing towards a point is equal to the sum of currents flowing away form it.

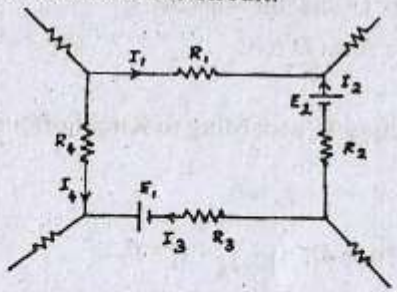
For example let a number of conductors meet at a junction as shown in figure. Let I_1, I_2, I_3, I_4 and I_5 be currents flowing. Generally the currents flowing towards the points are taken as positive whereas the currents flowing away from the points are taken as negative. Ac- cording to first law,



$$I_1 - I_2 + I_3 - I_4 + I_5 = 0 \text{ or } I_1 + I_3 + I_5 = I_5 + I_4$$

The first law is based on the principle that in an electric circuit, at any point the charge cannot be accumulated.

(ii) Kirchhoff s Second Law: In a closed path of networks of conductors, the algebraic sum of the products of resistance and current of each part of the closed path is equal to the algebraic sum of e.m.fs in the circuit.



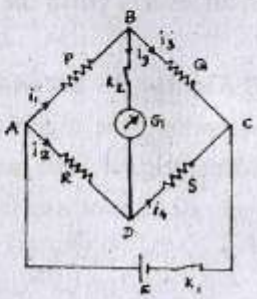
Consider a closed loop of circuit ABCDA as shown in figure. In the circuit the current which flows in the clockwise direction is taken as positive and the current which flows in the anticlockwise direction is taken as negative. Also e.m.fs which sents current in the clockwise direction are taken as positive and those that send current in the anticlockwise direction as negative.

Applying Kirchhoff s second law to the circuit in figure, we get $I_1 R_1 - I_2 R_2 + I_3 R_3 - I_4 R_4 = E_1 - E_2$

c. Wheatstone Bridge:

Wheatstone bridge consists of four resistances P, Q,R and S connected as shown in figure. A galvanometer A of a resistance G is connected between the points B and D and a

cell is connected between the Points A and C. Two keys are also connected in the circuit as shown. When the keys are closed, a current flows in the circuit. Current from the cell is divided into two parts at A.



The current i_1 flows through P and the current i_2 flows through the galvanometer. The current i_3 through Q flow from B to C and the current i_4 through S flows form D to C.

At the junction B, according to Kirchhoff's first raw,

$$i_1 - i_g - i_3 = 0 \qquad (1)$$

At the junction D, $i_2 - I_g - i_4 = 0$ (2)

The bridge is said to be balanced if there is no flow of current through the galvanometer. For this the resistances are adjusted such that there is no deflection in the galvanometer.

$$\therefore I_g = 0 \qquad (3)$$

Hence from equation (1) and (2)

$$i_1 - i_3 = 0 \quad \text{or} \quad i_1 = i_3 \qquad (4)$$

$$i_2 - i_4 = 0 \quad \text{or} \quad i_2 = i_4 \qquad (5)$$

Applying Kirchhoff's second law to the closed path ABDA, we get

$$i_1P + i_gG - i_2R = 0$$

In the closed path BCDB,

$$i_3Q - i_4S - I_gG = 0$$

When $i_g = O$, equation (6) and (7) reduce to

$$i_1P = i_2R$$

$$i_3Q = I_4S$$

Dividing the equations (S) and (9) we get

$$\frac{i_1P}{i_3Q} = \frac{I_2R}{i_4S}$$

But $i_1 = i_3$ and $i_2 = i_4$

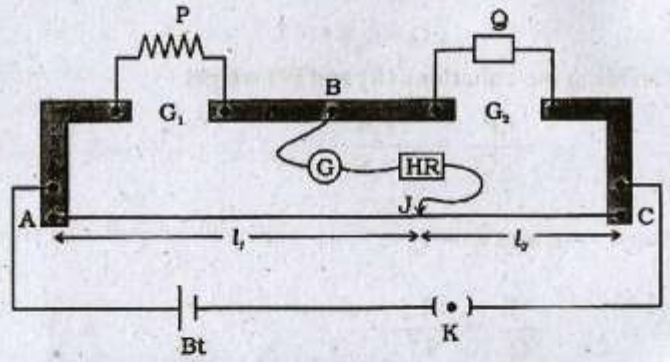
$$\therefore \quad \frac{P}{Q} = \frac{R}{S}$$

This is the condition of a balanced Wheatstone bridge. If the value of the resistances P,Q and R are known , the value of S can be calculated. Thus the principle of wheatstone's bridge is used for the determination of unknown resistances. Metre Bridge, post office Box and Carey Foster's Bridge work on this principle.

d. Metre bridge

Metre bridge is one form of Wheatstone's bridge. It consists of thick strips of copper, of negligible resistance, fixed to a wooden board. There are two gaps G_1 and G_2 between these strips. A uniform manganin wire AC of length one metre whose temperature coefficient is low, is stretched along a metre scale and its ends are soldered to two copper strips. An unknown resistance P is connected in the gap G1 and a standard

resistance Q is connected in the gap G_2 (Figure). A metal jockey J is connected to B through a galvanometer (G) and a high resistance (HR) and it can make contact at any point on the wire AC. Across the two ends of the wire, a Leclanche cell and a key are connected.



Metre bridge

Adjust the position of metal jockey on metre bridge wire so that the galvanometer shows zero deflection. Let the point be J. The portions AJ and JC of the wire now replace the resistances R and S of Wheatstone's bridge. Then

$$\frac{P}{Q} = \frac{R}{S} = \frac{rAJ}{rJC}$$

where r is the resistance per unit length of the wire.

$$\frac{P}{Q} = \frac{AJ}{JC} = \frac{l_1}{l_2}$$

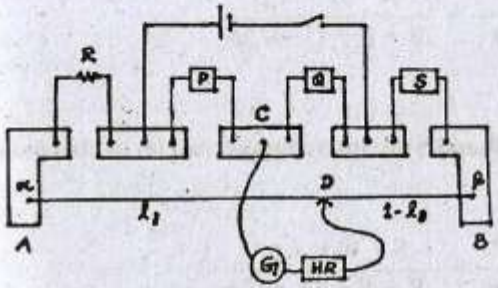
where $AJ = l_1$ and $JC = l_2$

$$P = Q\,\frac{l_1}{l_2}$$

Though the connections between the resistances are made by thick copper strips of negligible resistance, and the wire AC is also soldered to such strips a small error will occur in the value of l_1/l_2 due to the end resistance. This error can be eliminated, if another set of readings are taken with P and Q interchanged and the average value of P is found, provided the balance point J is near the mid point of the wire AC.

e. Carey Foster's Bridge

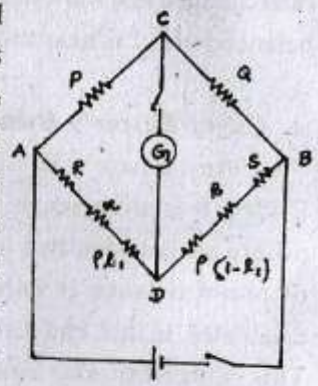
Carey Foster's Bridge is the improved form of Metre Bridge. It is more sensitive using this, we can determine the difference between two nearly equal resistances. If the value of one resistance is known, the value of the other can be calculated. In this, end resistances are eliminated in calculation. This bridge can also be used to measure accurately a given very low resistances.



It consists of a straight uniform wire of managing exactly one metre long (AB). The wire is stretched on a wooden board. The ends A and B are joined to thick copper strips of low resistance as shown is figure. Between in these two copper strips, three copper strips are fixed such that there are four gaps in the wooden board. A meter scale is fixed on the board parallel to the wire.

Two equal resistance P and Q are connected in the inner gaps and the resistances R and S are connected in the outer gaps. The cell and galvanometer are connected as shown in fig. Using a jockey,. contact can be made al any point on the wire AB.

Let α and β be the end resistances at the ends A and B respectively. Let ρ be the resistance per unit length. The resistance R is in left gap and S in the right gap. Now let l_1 be the balancing length. In this condition, the equivalence Wheatstone bridge is as shown in figure. When the bridge is balanced.



$$\frac{P}{Q} = \frac{R + \alpha + l_1\rho}{S + \beta + (1 - l_1)\rho}$$

Now R and S are interchanged and let the balancing length be l_2.

$$\frac{P}{Q} = \frac{S + \alpha + l_2\rho}{R + \beta + (1 - l_2)\rho}$$

Comparing equation(1) and (2) we get

$$\frac{R + \alpha + l_2\rho}{S + \beta + (1 - l_1)\rho} = \frac{S + \alpha + l_2\rho}{R + \beta + (1 - l_2)\rho}$$

Adding 1 on both side, we get

$$\frac{R + \alpha + l_1\rho + S + \beta + (1 - l_1)\rho}{S + \beta + (1 - l_1)\rho} = \frac{S + \alpha + l_2\rho + R + \beta + (1 - l_2)\rho}{R + \beta + (1 - l_2)\rho}$$

$$\therefore \quad \frac{R + S + \alpha + \beta + \rho}{S + \beta + (1 - l_1)\rho} = \frac{R + S + \alpha + \beta + \rho}{R + \beta + (1 - l_2)\rho}$$

$$\therefore \quad S + \beta + (1 - l_1)\rho = R + \beta + (1 - l_2)\rho$$

$$\text{or} \quad S - l_1\rho = R - l_2\rho$$

$$\therefore \quad R - S = \rho(l_2 - l_1)$$

$$\therefore \quad R = S + \rho(l_2 - l_1)$$

Knowing ρ, l_1 and l_2, (R – S) can be calculated. If S is known R can be calculated.

Determination of ρ:

To determine the resistance per unit length of the bridge wire, the resistance R is replaced by a copper strip (R = O). Now we have to find the balancing length and let it be l_2. Now keeping S in the left gap and copper strip in the right gap, we have to find the balancing length. Let it be l_2. The values of P and Q should be equal.

$$R = S + \rho(l_2 - l_1)$$

Here $R = 0$

$$\therefore \quad \rho = \frac{S}{(l_1 - l_2)}$$

The experiment is repeated for different values of S. The mean value of ρ is calculated. Using the value of ρ in equation (5), the resistance R can be calculated.

POTENTIOMETER

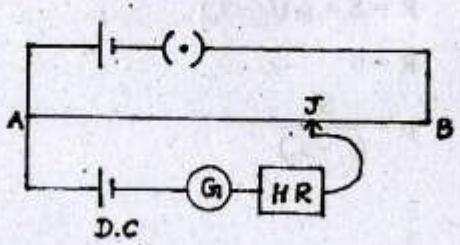
Potentiometer is a device which is used to measure potential difference accurately. It is also used to measure current.

Construction

It consists of ten segment of a uniform wire of magnanin or constantan, each one metre long. The segments are stretched parallel to each other on a horizontal wooden board. The ends of the wires are connected to copper strips of zero resistance. The ends are fitted with binding screws for connection. Using a movable jockey contact can be made at any point of the wire. A metre scale is fixed on the wooden board parallel to the segment of the wire.

Principle of Potentiometer

The principle of the potentiometer can be explained using the circuit shown in figure. In the figure AB represents the wire of the potentiometer. A and B are connected to a battery of steady emf. When the key in this circuit is closed a steady current flows through the wire of the potentiometer. This circuit is called the primary circuit.



The positive end of the Daniel cell is connected to the end A of the potentiometer. The negative end is connected to the jockey through a high resistance and a galvanometer. This circuit is called the secondary circuit. The positive end of cell is connected to the end A. Hence the current due to this circuit flows in a direction opposite to that of the current due to the primary circuit. Hence the e.m.f of the cell opposes the p.d between the ends of the potentiometer wire, when the jockey makes contact at any point of the wire.

Using the jockey, let the contact be made at the point J on the potentiometer. If the p.d between the points A and J is greater than the e.m.f of the cell in the secondary, the deflection of the galvanometer will be in the right and side. On the other hand, if the p.d between the points A and J is less, the deflection will be in the refthand side. The jockey is moved on the potentiometer wire such that there is no deflection in the galvanometer. In this case the p.d between the point A and the point of contact of jockey on the wire is exactly equal to the e.m.f of the cell in the secondary. In that case the point J is called the balancing point and the length AJ is called balancing length. Let the balancing length be l. If i is the current through the potentiometer wire and ρ is the resistance per unit length, the p.d across AJ is $I \rho l$.

If E is the e.m.f of the secondary cell, then

$$E = i \rho l \qquad \text{- (1)}$$

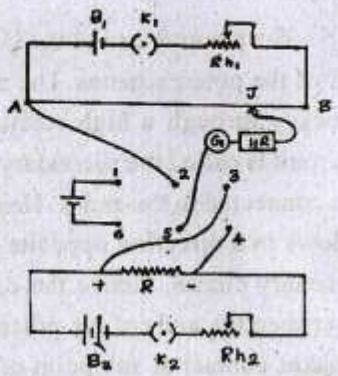
Since ρ and i are constants,

$$E \alpha l \qquad \text{- (2)}$$

Thus is the principle of the potentiometer.

a. Measurement of current

For the measurement of current using a potentiometer the circuit is as shown is figure.



The ends of the Potentiometer A and B are connected to an accumulator Bt, through a key K_1, and a rheostat Rh_1. This is the primary circuit.

In the secondary, a six terminal key is used. Using this, the two p.d may be included with the potentiometer circuit separately. The middle pair of terminal 2 and 5 are connected to the end A and the jockey through a galvanometer G and a high resistance. A Daniel cell of e.m.f 1.08 volt is connected across the terminals 1 and 6. A battery 82, key K_2, rheostat Rh_2 and a standard resistance R are connected in series. The positive end of the standard resistance is connected to the terminal 3 and the negative end to 4 as shown in figure.

First including the Daniel cell in the potentiometer, the balancing length is determined. Let the balancing length be l_0 According to the principle of potentiometer.

$$1.08 \propto l_0 \qquad \text{- (1)}$$

Next the p.d across the standard resistance R is included in the main circuit and the balancing length / is determined. If i is the current flow through the standard resistance, the p.d across R is i R.

$$\therefore \quad i R \propto l \qquad \text{- (2)}$$

Dividing equation (2) by equal (1), we get

$$\frac{iR}{1.08} = \frac{l}{l_0} \qquad \text{- (3)}$$

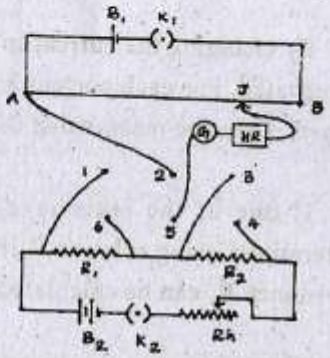
$$\therefore i = \frac{1.08}{R} = \frac{l}{l_0} \qquad \text{- (4)}$$

Using equation (4), the current in the circuit can be calculated

b. Measurement of resistance

To compare the given two resistances, the circuit is as shown in figure. If one of the resistance is known, the other resistance can be calculated.

In the secondary circuit, a six terminal key is used. Using this, the two p.d may be included with the potentiometer separately. The middle pair of the terminals 2 and 5 are connected to the end A and jockey through a galvanometer and high resistance.



Two resistances R_1 and R_2 which are to be compared are connected in series with a battery B_2, key K_2 and a rheostai Rh. The ends of the resistances R_1 and R_2 are connected to the six terminal key as shown in fig. When the key K_2 is closed, a steady current i flows through the resistances R_1 and R_2. The p.d across them will be i R_1 and i R_2.

First the p.d across R_1 is included in the potentiometer circuit and the balancing length is found. Let it be l_1. According to the principle of potentiometer,

$$\therefore \quad i R_1 \propto l_1 \qquad \text{- (1)}$$

Next the p.d across R_2 is included and the balancing length is found. Let it be l_1.

$$\therefore \quad i R_2 \propto l_2 \qquad \text{- (2)}$$

Dividing equation (1) by (2) we get

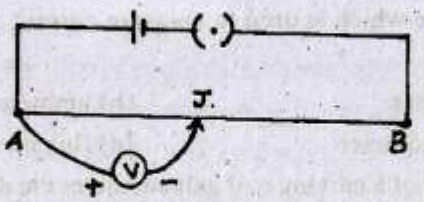
$$\frac{R_1}{R_2} = \frac{l_1}{l_2} \qquad \text{- (3)}$$

By changing the current in the secondary the experiment is repeated. For each current R_1/R_2 is calculated as described above. Then the mean value of R_1/R_2 is calculated.

If one of the resistance is known, the other can be determined using relation $R_1/R_2 = l_1 / l_2$. If R_1 is known, the resistance R_2 can be calculated using the relation.

c. Calibration of low range voltmeter

The ends of the potentiometer A and B are connected to a battery of steady e.m.f. The positive end of the Daniel cell is connected to the end A and the negative to the jockey through a galvanometer and a high resistance. Now the balancing length is found. Let it be l_0. The fall of potential per unit length of the potentiometer wire is $1.08/ l_0$ volt.



The secondary circuit is replaced by a voltmeter. The positive end of the voltmeter is connected to the end A and the negative to the jockey (figure). The jockey is pressed along the wire so that the voltmeter gives a reading V volt. The length of the wire AJ is found.

Let it be l. The p.d between A and J is equal to $1.08/l_0 \times l$ volt.

$$\therefore \text{ Correction } = ((1.08/l_0)\, l - V)$$

The experiment may be repeated for different value of the voltmeter such as 0.1,0.2....etc. For each voltmeter reading correction may be calculated. By taking the voltmeter reading along the x- axis and correction along Y-axis , a calibration graph may be drawn.

Model Questions

1. The sensitivity of the Wheatstone bridge is maximum when
   (a) P/Q = R/X (b) R = X, P = O
   (c) P = Q = R = X = G (d) none of the above
2. While using a Wheatstone's bridge
   (a) both the keys should be pressed
   (b) battery key should be pressed first
   (c) galvanometer key should be pressed first
   (d) any key may be pressed

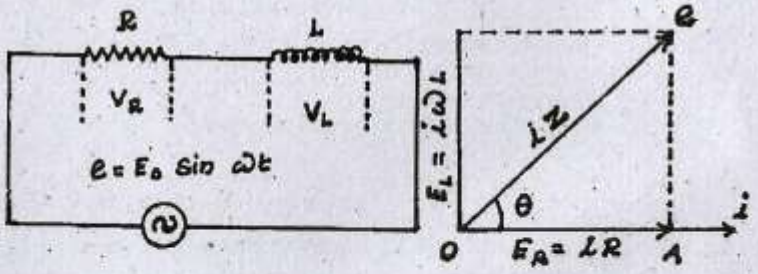
UNIT - II
ALTERNATING CURRENT

A.C CIRCUITS WITH DOUBLE COMPONENTS

(a) A.C Circuit having inductance and resistance

An alternating e.m.f $e = E_0 \sin \omega t$ is applied across a circuit containing a resistance R and an inductance L. (fig. 5-10). If i is the instantaneous current, the p.d across R is $E_R = R\,i$ and the p.d across the inductance is E_L - $i\omega L$.

The p.d across the resistance is in phase with the current through the resistance. The p.d across the inductance leads the current through the inductance by an angle $\pi/2$. The current in the circuit is the same at any point. Hence current is taken as the reference axis. A vector voltage diagram is drawn (fig 5-11) where the vector OA represents the magnitude and direction of the p.d across the resistance. The vector OB represents the p.d across the inductance both in magnitude and direction. The resultant vector OC will represent the effective p.d across the inductance and the resistance in series.



$$\therefore \text{OC} = \sqrt{OA^2 + OB^2}$$

$$\text{ie} \quad e = \sqrt{E_R^{\,2} + E_L^{\,2}}$$

$$= i\sqrt{R^2 + (L\omega)^2}$$

$$\therefore \quad i = \frac{e}{\sqrt{R^2 + (L\omega)^2}} \qquad \text{- (1)}$$

The term $\sqrt{R^2 + (L\omega)^2}$ is called impedance of the circuit and measured in the unit of ohm. It is denoted by the letter Z.

$$\therefore Z = e/i = \sqrt{R^2 + (L\omega)^2} \qquad \text{- (2)}$$

From the vector diagram

$$\tan \theta = AC/OA = \omega L/R \qquad \text{- (3)}$$

tan θ is positive. This shows that the current lags behind the applied e.m.f by a phase angle θ where

$$\theta = \tan^{-1}(\omega L/R) \qquad \text{- (4)}$$

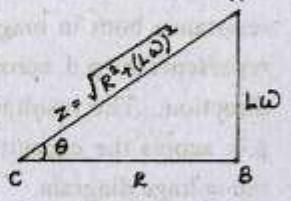
Hence the current at any instant of time is

$$i = \frac{e_0}{\sqrt{R^2 + (L\omega)^2}} \sin(\omega t + \theta) \qquad \text{- (5)}$$

The peak value of current $i_0 = \dfrac{e}{\sqrt{R^2 + (L\omega)^2}} \sin(\omega t + \theta)$ - (6)

$$i = i_0 \sin(\omega t + \theta) \qquad \text{- (7)}$$

A triangle whose sides are proporitonal to R, ωL and Z is called the impedence triangle. The impedence triangle is as shown in figure. The hypotenuse will repreent the impedence of the circuit and ∠ACB gives the phase lag of the current behind the voltage.

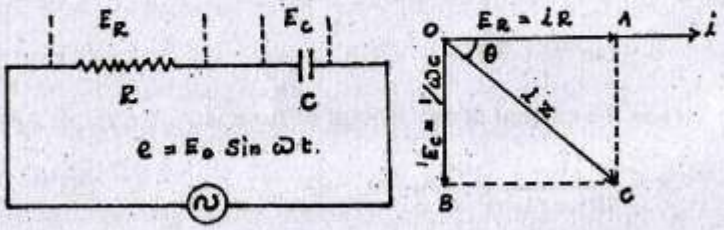


The reciprocal of teh impedence is clled the admittance of the circuit and is denoted by the letter Y.

$$Y = \frac{1}{Z} = \frac{e}{\sqrt{R^2 + (L\omega)^2}} \text{ mho} \qquad \text{- (8)}$$

b. A.C. circuit having resistance and capacitance

An alternating e.m.f $e = E_o \sin \omega t$ is applied across a resistance R and a condenser of capacity C connected in series (figure). If i is the instantaneous current, the p.d across the resistance is $E_R = R\,i$ and the p.d across the capacitor is $E_C - i/\omega C$.



The p.d across the resistance is in phase with the current through the resistance. The p.d across the inductance leads the current through the inductance by an angle $\pi/2$. The current in the circuit is the same at any point. Hence current is taken as the reference axis. A vector voltage diagram is drawn (figure) where the vector OA represents the p.d. across the resistance both in magnitude and direction. the vector OB repersents the p.d. across the capacitor both in magnitude and direction. The resultant vector OC represents the effective p.d. acorss the capacitor and the resistance in series. From the voltage diagram.

$$OC = \sqrt{OA^2 + OB^2}$$

ie $$e = \sqrt{E_R^2 + E_C^2}$$

$$= i\sqrt{R^2 + (1/(C\omega)^2)}$$

$$\therefore \quad i = \frac{e}{\sqrt{R^2 + (1/(C\omega)^2)}} \qquad \text{- (1)}$$

The term $\sqrt{R^2 + (1/(C\omega)^2)}$ is called impedance of the circuit.

$$\therefore \text{ Impedence } Z = e/i = \sqrt{R^2 + (1/(C\omega)^2)} \qquad \text{- (2)}$$

From the vector diagram

$$\tan\theta = AC/OA = -1/(C\omega)^2 \qquad \text{- (3)}$$

Tan θ is negative. This shows that the current lead the applied e.m.f by a phase angle θ where

$$\theta = \tan^{-1}(1/(C\omega)^2) \qquad \text{- (4)}$$

Hence the current at any instant of time is

$$i = \frac{e_o}{\sqrt{R^2 + (1/(C\omega)^2)}} \sin(\omega t + \theta) \qquad \text{- (5)}$$

The peak value of current $i_o = \dfrac{e}{\sqrt{R^2 + (1/(C\omega)^2)}}$ - (6)

$$i = i_o \sin(\omega t + \theta) \qquad \text{- (7)}$$

The admittance of the circuit is

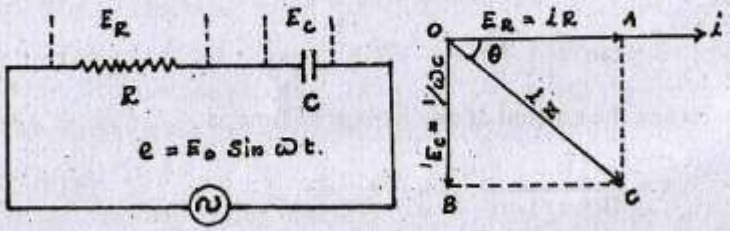
$$Y = \frac{1}{Z} = \frac{e}{\sqrt{R^2 + (1/(C\omega)^2)}} \text{ mho} \qquad \text{- (8)}$$

The reciprocal of teh impedence is clled the admittance of the circuit and is denoted by the letter Y.

$$Y = \frac{1}{Z} = \frac{e}{\sqrt{R^2 + (L\omega)^2}} \text{ mho} \qquad \text{- (8)}$$

b. A.C. circuit having resistance and capacitance

An alternating e.m.f $e = E_o \sin \omega t$ is applied across a resistance R and a condenser of capacity C connected in series (figure). If i is the instantaneous current, the p.d across the resistance is $E_R = R\,i$ and the p.d across the capacitor is $E_C - i/\omega C$.



The p.d across the resistance is in phase with the current through the resistance. The p.d across the inductance leads the current through the inductance by an angle $\pi/2$. The current in the circuit is the same at any point. Hence current is taken as the reference axis. A vector voltage diagram is drawn (figure) where the vector OA represents the p.d. across the resistance both in magnitude and direction. the vector OB repersents the p.d. across the capacitor both in magnitude and direction. The resultant vector OC represents the effective p.d. acorss the capacitor and the resistance in series. From the voltage diagram.

$$OC = \sqrt{OA^2 + OB^2}$$

ie $$e = \sqrt{E_R^2 + E_C^2}$$

$$= i\sqrt{R^2 + (1/(C\omega)^2)}$$

$$\therefore \quad i = \frac{e}{\sqrt{R^2 + (1/(C\omega)^2)}} \qquad \text{- (1)}$$

The term $\sqrt{R^2 + (1/(C\omega)^2)}$ is called impedance of the circuit.

$$\therefore \text{ Impedence } Z = e/i = \sqrt{R^2 + (1/(C\omega)^2)} \qquad \text{- (2)}$$

From the vector diagram

$$\text{ton } \theta = AC/OA = -1/(C\omega)^2 \qquad \text{- (3)}$$

Tan θ is negative. This shows that the current lead the applied e.m.f by a phase angle θ where

$$\theta = \tan^{-1}(1/(C\omega)^2) \qquad \text{- (4)}$$

Hence the current at any instant of time is

$$i = \frac{e_0}{\sqrt{R^2 + (1/(C\omega)^2)}} \sin(\omega t + \theta) \qquad \text{- (5)}$$

The peak value of current $i_o = \dfrac{e}{\sqrt{R^2 + (1/(C\omega)^2)}}$ - (6)

$$i = i_o \sin(\omega t + \theta) \qquad \text{- (7)}$$

The admittance of the circuit is

$$Y = \frac{1}{Z} = \frac{e}{\sqrt{R^2 + (1/(C\omega)^2)}} \text{ mho} \qquad \text{- (8)}$$

4. A 2000 ohm resistor and a 1 μf capacitor are connected in series across a 120 volts (r.m.s) 60 cyclesisec line (a) what is the impedence (b) what is the r.m.s value of the current (c) what will be the reading of an a.c voltmeter connected across the resistor and across the capacitor?

a Impedence $Z = \sqrt{R^2 + (1/(C\omega)^2)}$

Here $R = 2000$ ohm $= C = 1\mu f = 1 \times 10^{-6}$ f

$\omega = 2\pi f = 2 \times 3.14 \times 60 = 376.8]$

$\therefore \quad C\omega = 376.8 \times 10^{-6}$

$\therefore \quad Z = \sqrt{(2000)^2 + (10^{12}/(376.8)^2)}$

$= 10^3\sqrt{4 + 7.043} = 10^3\sqrt{11.043}$

$Z = 3323.15$ ohm

b. $I_{r.m.s} = \frac{e}{Z} = \frac{120}{3323.15} = 0.0361$ A

c. ρ.d. across the resistance

$E_R = I_{r.m.s} \times R = 0.0361 \times 2000 = 72.2$ volt

p.d. across the capacitor

$E_C = I_{r.m.s} \times X_C = I_{r.m.s} \times (1/C\omega)$

$= 0.0361 \times (10^6/376.8)$

$= 0.0361 \times 2653.9 = 95.54$ volt

Thus a.c voltmeter will read 72.2 V across the resistor and 95.50 V across the capacitor.

Power in an a.c circuit

Power is defined as the rate of doing work. In the d.c circuit power is the product of current and voltage. If the current

is in ampere and voltage in volt, then the power is expressed in watt. In the case of a.c circuit, e and i vary continuously. So in a.c circuit, we have to calculate the work done at any instant of time and then the power for the complete cycle is calculated.

(a) Power in a Pure Resistive Circuit:

Let an alternating e.m.f be applied to a circuit containing only R. At any instant of time let $e = E_o \sin \omega t$ be the instantaneous value of the applied voltage and $i = I_o \sin \omega t$ be the instantaneous current.

$\therefore$ Power at that instant $= e \; i$

$= E_o I_o \sin^2 \omega t \qquad -(1)$

The average power dissipated during a complete cycle is

$$P = \frac{1}{T} \int_0^T E_o I_o \, 2 \sin^2 \omega t \, dt$$

$$P = \frac{E_o I_o}{2T} \int_0^T 2 \sin^2 \omega t \, dt$$

$$P = \frac{E_o I_o}{2T} \int_0^T (1 - \cos 2\omega t) \, dt$$

$$= \frac{E_o I_o}{2}$$

$$P = \frac{E_o}{\sqrt{2}} \quad \frac{I_o}{\sqrt{2}}$$

But we know that $E_o/\sqrt{2}$ is the r.m.s value of voltage and $I_o/\sqrt{2}$ is the r.m.s value of current.

$\therefore$ Average power $P = E_{r.m.s} \; I_{r.m.s}$

b. Power in inductive circuit

Let an alternating e.m.f be applied to a circuit containing only inductance L. The current through a pure inductance lags behind the applied e.m.f in phase by $\pi/2$.

$$\therefore \quad e = E_0 \sin \omega t$$
$$i = I_0 \sin (\omega t - \pi/2)$$

$\therefore$ Instantaneous power = ei

$$= E_0 I_0 \sin \omega t \, - \sin (\omega t - \pi/2)$$
$$= - E_0 I_0 \sin \omega t \, - \cos \omega t$$
$$= - \frac{E_0 I_0}{2} \sin 2\omega t$$

$\therefore$ Average power over one cycle is

$$P = \frac{1}{T} \int_0^T \frac{E_0 I_0}{2} \sin 2\omega t - dt$$
$$= \frac{E_0 I_0}{2T} \int_0^T \sin 2\omega t - dt$$

But $\int_0^T \sin 2\omega t - dt = 0$

$\therefore$ Average Power P = 0

Thus power dissipation in a pure inductance is zero and the current in such a circuit is known as wattless current. The choke coil works on this principle.

c. Power in capacitive circuit

Let an alternating e.m.f be applied to circuit containing only capacitance C. The current through a pure capacitor leads the applied e.m.f in Phase by $\pi/2$.

$$\therefore e = E_0 \sin \omega t$$
$$i = I_0 \sin (\omega t + \pi/2)$$

$\therefore$ Instantaneous Power = e i

$$= E_0 I_0 \sin \omega t - \sin(\omega t + \pi/2)$$
$$= E_0 I_0 \sin \omega t - \cos \omega t$$
$$= \frac{E_0 I_0}{2} \sin 2\omega t$$

As the average of sin 2 ωt over a cycle is zero. Hence the average power is zero. Thus the average Power dissipation in a pure capacitance circuit is zero. Hence the current through it also wattless or idle.

d) Power in a circuit containing L and R in series

Let an alternating e.m.f be applied to a circuit containing an inductance L and a resistance R. At any instant of time let $e = E_0 \sin \omega t$ and $i = I_0 \sin (\omega t - \theta)$ where θ is the phase lag of the current behind the applied e.m.f.

Instantaneous Power = e i

$$= E_0 I_0 \sin \omega t - \sin (\omega t - \theta)$$
$$= E_0 I_0 \sin \omega t \, [\sin \omega t \cos \theta - \cos \omega t - \sin \theta]$$
$$= E_0 I_0 \, [\sin^2 \omega t - \cos \theta - \sin \omega t - \cos \omega t - \sin \theta]$$
$$= E_0 I_0 \sin^2 \omega t - \cos \theta - \frac{E_0 I_0}{2} - \sin \omega t - \sin \theta$$

Average power in a complete cycle is

$$P = \frac{1}{T} \int_0^T E_0 I_0 \cos \theta - \sin^2 \omega t - dt$$
$$- \frac{1}{2} \int_0^T E_0 I_0 \sin \theta - \sin 2\omega t - dt$$
$$= \frac{E_0 I_0 \cos \theta}{T} \int_0^T \sin^2 \omega t - dt - \frac{E_0 I_0 \cos \theta}{2T} \int_0^T \sin 2\omega t - dt$$

But $\int_0^T \sin^2 \omega t - dt = \frac{1}{2}$

$$\int_0^T \sin 2\omega t - dt = 0$$

$$\therefore \text{Power } P = \frac{E_o I_o}{2} - \cos\ \theta$$

$$= \frac{E_o I_o}{2} \cos\ \theta$$

$$P = \frac{E_o}{\sqrt{2}} - \frac{I_o}{\sqrt{2}} \cos\ \theta$$

$$\therefore P = E_{r.m.s}\ I_{r.m.s}\ \cos\ \theta$$

It is clear that power depends that not only on the r.m.s value of voltage and current but also on the cosine of the angle of lag between the current and voltage. Hence cos θ is known as the power factor and $\theta = \tan^{-1}(L\omega/R)$

$$\therefore \text{Power factor } \cos\theta = \frac{R}{\sqrt{R^2 + (L\omega)^2}}$$

$$\text{Power factor} = \frac{\text{Resistance}}{\text{Impedence}} = \frac{R}{Z}$$

The product $E_{r.m.s}\ I_{r.m.s}$ is known as the apparent power.

$$\therefore \text{Power Factor} = \frac{\text{The power}}{\text{Apparent power}}$$

∴ True power = Power factor x Apparent power

In a similar way, we can show that the power in a circuit containing R and C is $E_{r.m.s}\ I_{r.m.s} \cos\theta$

$$\therefore \text{Power factor } \cos\theta = \frac{R}{\sqrt{R^2 + ((1/(C\omega)^2)}}$$

e. Wattless current

If an a.c circuit is purely inductive or purely capacitive, the phase angle is π/2. Hence cos θ = 0. Therefore the power consumed in such a circuit is zero. The current in such a circuit does not perform any useful work. So it is called wattless or idle current. In this the circuit does not consume any power. But it offers a resistance to the flow of alternating current. This is the principle of choke.

f. Choke

For many purposes, it is required to reduce the current in a given circuit with a minimum waste of power. In a d.c circuit, it is achieved by using a resistance in the circuit. The power loss in this circuit is I^2R.

In an a.c circuit, when a resistance is used, the wastage of energy is I^2R. In order the avoid any wastage of energy, an inductance coil is used. If the resistance of the choke is r and the inductance of the choke coil is L, then the power factor $\cos\theta = r/\sqrt{r^2 + L^2\omega^2}$. In the case of pure inductance having no resistance cos θ is equal to zero and the power consumed is zero. Hence an inductance coil of very small resistance used to control the current in an a.c circuit is called a choking coil or choke.

A choke consists of a coil of several turns of insulated wire of low resistance, but large inductance, wound over a laminated core. The core is layered and is made up of thin sheets of stalloy to reduce hysteresis losses. The laminations are coated with shillac to irsulate and bound together firmly so as to minimise loss of energy due to eddy currents. When used

in an a.c circuit, the current through lags behind the choke the e.m.f by $\pi/2$. Hence there is no dissipation of power. The wastage of power is due to the Joule heating in the co, to its resistance and eddy current and hysteresis loss in the core. These are reduced to a minimum.

Choke coils which are used on low frequency current have iron core. These are known as row frequency or audio frequency chokes. Choke coils which are used on high frequency, have air core. These are known as high frequency or radio frequency chokes.

Problems

1. An alternating voltage of 10 volts at 100 cps is applied to a choke of inductance 5H and of resistance 200 ohm. Find the power factor of the coil and the power absorbed.

Solution

$$\therefore \text{ Power factor } \cos\theta = \frac{R}{\sqrt{R^2 + (L\omega)^2}}$$

Here $R = 200$ ohm ; $L = 5$ H

$$\omega = 2\pi f = 2 \times 3.14 \times 100 = 628$$

$$\therefore \text{ Power factor } = \frac{200}{\sqrt{200^2 + (628 \times 5)^2}}$$

$$= \frac{200}{3146.36}$$

$$= 0.063$$

Power Factor $= 0.063$

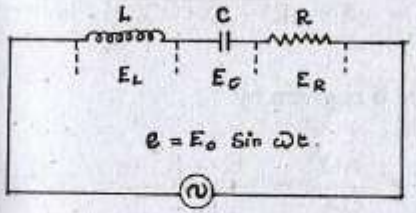
Power absorbed $= E_{r.m.s}\ I_{r.m.s} \cos\theta$

$$= 10 \times \frac{10}{\sqrt{200^2 + (2\pi \times 100 \times 5)^2}} \times 0.063$$

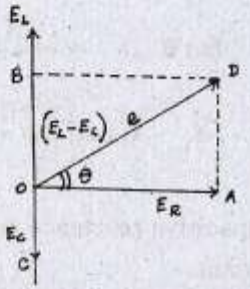
$$= 0.002 \text{ watt}$$

A.C. Circuit having L, C and R

An alternating e.m.f $e = E_0 \sin \omega t$ is applied to a circuit containing a resistance R, inductance L and a capacitance C. (Fig 5-15). If i is the instantaneous current, the p.d across R is $E_R = R\,I$, the p.d across L is $E_L = i.X_L$ and the p.d across C is $E_C = i\,X_L$



The voltage drop across the resistance is in phase with the current, the voltage drop across the inductance is reading the current by a phase angle $\pi/2$ and the voltage drop across the capacitance is lagging the current by a phase angle $\pi/2$.



The resultant voltage can be calculated by drawing the vector diagram. The current in each of the component is the same. Hence the current is taken as the reference axis. The vector diagram of the r.m.s values of the potential drops E_L, E_C and E_R across the respective components is illustrated in figure in which oA represents E_R. The sum of E_L and E_C is given by

$(E_L - E_C)$ since the vectors are oppositely drawn. It is represented by OB in the fig. The diagonal OD represents the p.d across the whole circuit. From the figure.

$$e^2 = E_R^2 + (E_L - E_C)^2$$

$$e = \sqrt{i^2R^2 + i^2(X_L - X_C)^2}$$

$$e = i\sqrt{R^2 + (X_L - X_C)^2}$$

$$i = \frac{e}{\sqrt{R^2 + (X_L - X_C)^2}}$$

Impedence $Z = e/I = \sqrt{R^2 + (X_L - X_C)^2}$

The phase angle θ is given by

$$\tan\theta = \frac{AO}{OA} = \frac{E_L - E_C}{E_R}$$

$$\tan\theta = \frac{X_L - X_C}{R}$$

$(X_L - X_C)$ or $\left[L\omega - \frac{1}{C\omega}\right]$ is the sum of the inductive and capacitive reactance and or is called the impedence of the circuit.

Gives the phase relation between the current and the applied e.m.f. The current leads or lags the e.m.f depending upon the magnitude of $L\omega$ and $1/C\omega$.

Case 1 : when $L\omega > 1/C\omega$

$$\theta = \tan^{-1}\left[\frac{L\omega - (1/C\omega)}{R}\right]$$

In this case $\tan\theta$ is positive. Hence θ is positive. Therefore the current lags behind the applied e.m.f.

$$\therefore i = i_o \sin(\omega t - \theta)$$

Case 2 : when $L\omega < 1/C\omega$

$$\theta = \tan^{-1}\left[\frac{((1/C\omega) - LW)}{R}\right]$$

Since $\omega L < 1/C\omega$, θ is negative. Hence the current leads the voltage by an angle θ.

$$\therefore i = i_o \sin(\omega t + \theta)$$

When $L\omega = 1/c\omega$, θ becomes zero. In this case the current in the circuit is in phase with the applied e.m.f. The current is decided by the resistance.

8. Series Resonance Circuits

When an alternating e.m.f is applied to a circuit containing L, C and R in series, the peak value of current is given by

$$i_o = \frac{e}{\sqrt{R^2 + (L\omega - (1/c\omega)^2)}}$$

If the inductive reactance and the capacitive reactance are equal, i.e, $L\omega = 1/C\omega$ the impedence of the circuit is R.

The phase angle θ becomes zero and the applied e.m.f and the current will be in phase. The p.d. across the inductance and capacitance are equal in magnitude, but opposite in phase and therefore cancel out. The whole voltage is dropped across the resistance. Hence the circuit behaves as purely resistive circuit.

The peak value of current is e/R. When R is small, the current becomes very large. The current is in phase with the applied e.m.f. Now the circuit is said to be in resonance with the applied e.m.f. The circuit is said to be a series resonant circuit and the phenomenon of maximum current is called the resonance. Thus at resonance

$$L\omega = 1/C\omega$$
$$\omega^2 = 1/LC$$

(or)

$$\omega = 1/\sqrt{LC}$$

But frequency $f = \omega/2\pi$

$$\therefore \quad f = \frac{1}{2\pi\sqrt{LC}}$$

Here the frequency is called resonant frequency . The condition for resonance is that the frequency of the applied e.m.f must be equal to the natural frequency of the circuit, when the resistance in the circuit is negligible.

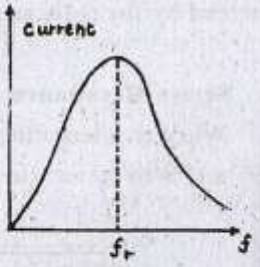
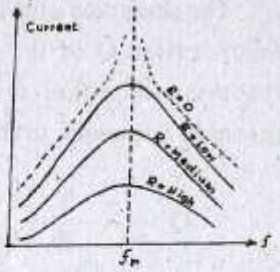


Figure. shows the variation of peak current with frequency for resonant circuit. At the natural frequency, the value of

current is maximum. When the incoming frequency is much lower or much higher than the natural frequency, the current in the circuit is very low. When the frequency approaches the resonant frequency f_r, the current begins to increase and reaches maximum at f_r. If the resistance of the circuit is small, the maximum current is higher.

Sharpness of a resonance

At the resonance, the current in the circuit is maximum and it is given by e/R. We can draw a graph between the amplitude of the current and the frequency. These curves are known as resonance curves. The curve is as shown in figure. The curve is drawn for three different resistances low, medium and high.



From the graph, it is clear that as the resistance in the circuit is reduced the resonant curve becomes sharper. The peak value of current shows that the circuit responds only to the frequency exactly equal to its natural frequency of the circuit f_r and to none others.

The resonance here is, therefore, said to be sharp. Thus sharpness of resonance is a measure of the rate of fall of amplitude from its maximum value at resonant frequency on either side of it. The more quickly the current amplitude fall for changes of frequency f_r, the sharper is said to resonance.

On the other hand, if the amplitude remains more or less at its peak value over an appreciable range of frequency on either side of resonant frequency, the circuit responds to a number of frequencies, near about f_r on either side of it. The resonance in this case is said to be flat. In ideal case when R = 0, the current is infinity at the resonance.

Q of a circuit:

The sharpness of resonance curve is determine by a quality factor called Q of the circuit. It is defined as the ratio of reactance of either the inductance or capacitance at the resonant frequency to the total resistance of the circuit. Thus

$$Q = \frac{X_L}{R} = \frac{L\omega}{R}$$

$$\text{or } Q = \frac{X_C}{R} = \frac{1}{C\omega R}$$

But at resonance, $X_L = X_C$. Hence we get the same value of Q from both expression. At resonance the current is inversely proportional to the resistance and directly proportional to e. Hence if e is large, the resonance curve is sharp.

Selectivity

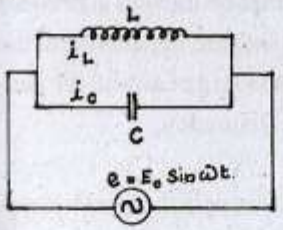
If the applied alternating voltage has a number of frequency components, the circuit will give maximum response only that frequency which has the frequency

$$\therefore \quad f = \frac{1}{2\pi\sqrt{LC}}$$

Thus out of number of frequencies it selects one frequency for which the current is maximum and for other frequencies the current is comparatively very small, in other words it shows selectivity. Hence this circuit is also called acceptor circuit.

b. Parallel Resonance Circuit

An inductance L of negligible resistance and a capacitor C are connected in parallel to an a.c supply. Let i_L be the current in the inductance. This will tag behind the applied e.m.f by $\pi/2$. Let i_c be the current in the condenser and it will lead the applied e.m.f by $\pi/2$. Therefore the current in the two branches differ in phase by π.



$$i_L = \frac{E_0}{\omega L} \text{ and } i_c = \frac{E_0}{1/\omega C} = E_0\,\omega C$$

The total current in the circuit will be the vector sum of the two currents:

$$\therefore \quad i = E_0\left[\frac{1}{\omega L} - \omega C\right]$$

If $i_L = i_C$, the resulting current from the a.c source is zero and the circuit is said to be in resonance and the frequency is known as the resonance frequency of the circuit.

At resonance,

$$i_L = i_C$$

$$\text{or } \frac{E_0}{\omega L} = E \cdot \omega C \quad \text{or } \frac{1}{\omega L} = \omega C$$

$$\therefore \omega^2 = \frac{1}{LC} \quad \text{or } \omega = \frac{1}{\sqrt{LC}}$$

But frequency $f = \frac{\omega}{2\pi}$

$$\therefore \quad f = \frac{1}{2\pi\sqrt{LC}}$$

Thus the parallel resonant frequency is the same as the frequency of the series resonant circuit. At the frequency f of the supply voltage, the circuit offers infinite impedance to the flow of the current so that no current is drawn from the supply. Such a circuit offering infinite impedence to the flow of current is called the parallel resonant circuit and the particular frequency is called the resonant frequency.

Thus the current through the parallel resonant circuit is zero and its works as a perfect choke for a.c. Here this circuit is called rejector circuit. Such circuits are used in wireless transmitter circuits and in filter circuits.

Problems

1. A resistance of 10 ohm is connected in series with an inductance of 0.5 henry. What capacitance must be connected in series with the combination to obtain maximum current? What will be the p.d across each element of circuit, if it is connected to 200V, 50 Hz mains?

Solution

When the current is maximum,

$$\omega L = \frac{1}{\omega C}$$

$$\therefore C = \frac{1}{\omega^2 L}$$

Here $L = 0.5$ H,

$\omega = 2\pi f = (2 \times 3.14 \times 50) = 314$

$$\therefore C = \frac{1}{0.5 \times (3.14)^2} = 0.00002024 \text{ F}$$

$$\therefore C = 20.24 \ \mu\text{F}$$

$$\text{current } I = \frac{V}{R} = \frac{200}{10} = 20 \text{ A}$$

p.d across $R = RI = 10 \times 20 = 200$ volt

p.d across L = p.d across $C = \omega LI$

$= 314 \times 50 \times 20 = 3410$ volts

2. A coil of resistance 100 ohm and inductance 0.5H is connected to a capacitor of 15 μf capacity across a 50 cycle, 200 V main supply. Calculate the reactance due to the inductance, reactance due to the capacitance, impedence, current and phase angle.

Solution

Inductive reactance $X_L = L\omega$

Here $L = 0.5$ H, $\omega = 2\pi f = 2 \times 3.14 \times 50 = 314$

$\therefore XL = 0.5 \times 314 = 157.0$ ohm

Capacitive reactance $X_C = \frac{1}{C\omega}$

Here $C = 15 \quad \mu f = 15 \times 10^{-6}$ f

$$\therefore X_C = \frac{10^6}{15 \times 314} = 0.00002123 \times 10^6 \text{ ohm}$$

$X_C = 212.30$ ohm

Impedence $Z = \sqrt{R^2 + (X_C - X_L)^2}$

$= \sqrt{100^2 + (212.3 - 157.6) \text{ sup } 2}$

$= 114.27$ ohm

19. What is the phase relation between current and voltage in an a.c. inductance circuit?
20. What is the unit of reactance?
21. What is the value of capacitive reactance?
22. What is the phase angle in an a.c. circuit having R and L?
23. What is power in a resistive circuit?
24. What is the power in inductive circuit?
25. What is the power in an L-R circuit?
26. What is the principle of choke coil?
27. What type of core is used in a radio frequency choke?
28. What is the impendence of L-C-R circuit?
29. What is peak value of current in a series resonant circuit?
30. What is the phase angle between the applied e.m.f. and the current at resonance?
31. What is the other name for series resonant circuit?
32. What is the other name for parallel resonant circuit?
33. What is the value of current in a parallel resonant circuit at resonance?

UNIT - III
NUMBER SYSTEMS, CODES AND LOGIC GATES

Number system

A number system is one which uses some code to represent the value of a number. In the number system we can use any type codes. The code which are in use have value according to their positions. Hence it is called positional number system. A number system is comprised of

1. A set of symbols for forming numbers.
2. A set of rules which may be used to form numbers from these symbols and assign values to them.
3. A set of rules for performing common arithmetic operation in this number system.

There are four types of number system which are often used in digital circuits. They are

1. Decimal 2. Binary 3. Octal 4. Hexadecimal

1. Decimal number system

The most familiar number system is the decimal system. In this system we are using ten symbols. They are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9. Since there are 10 symbols in this system, it is called decimal system. The base of this system is 10 because it uses ten codes. Using this code, we can form any number. The value of the digit depends upon its position. Since there are ten codes, the positional value of each digit will be the power of 10. The powers are numbered to the left of the decimal point starting with 0 and to the right of the decimal point starting with 1. The positional value of decimal number is given in the following table.

Left of the decimal point				Right of the decimal point		
10^3	10^2	10^1	10^0	10^{-1}	10^{-2}	10^{-3}
1000	100	10	1	0.1	0.01	0.001

For example consider the decimal number 7246.58. Thi can be written in the following way.

$$7 \times 10^3 + 2 \times 10^2 + 4 \times 10^1 + 6 \times 10^0 + 5 \times 10^{-1} + 8 \times 10^{-2}$$

$$= 7000 + 200 + 40 + 6 + 0.5 + 0.08$$

Hence the positional value of each digit is

$7 \rightarrow 7000, 2 \rightarrow 200, 4 \rightarrow 40, 6 \rightarrow 6, 5 \rightarrow 0.5, 8 \rightarrow 0.08$

b. Binary number system

A binary number system is a code that uses only two basi symbols. The symbols used in this system are 0 and 1. Hence th base of this system is 2. In this system also the value of the dig depends upon its position. The positional value of each digit will b the power of 2. The value will be as shown below.

Left of the decimal point					Right of the decimal point		
2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}
16	8	4	2	1	0.5	0.25	0.125

Using the above concept, we can form the binary number The decimal number and its binary equivalent is given in the decima binary table shown below.

Decimal	Binary
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111

Decimal to binary conversion

To convert the given decimal number into a binary number, the decimal number is repeatedly divided by 2 and the remainder in the reverse order is the binary equivalent of the decimal number.

Example : 1

Convert the decimal number 53 into a binary number.

2 | 53		
2 | 26	-	1
2 | 13	-	0
2 | 6	-	1
2 | 3	-	0
1	-	1

$[53]_{10} = [110101]_2$

Example – 2

Convert the decimal numbers 117 and 32 into binary numbers.

2	117						
2	58	-	1	2	32		
2	29	-	0	2	16	-	0
2	14	-	1	2	8	-	0
2	7	-	0	2	4	-	0
2	3	-	1	2	2	-	0
	1	-	1		1	-	0

$[117]_{10} = [1110101]_2$ $[32]_{10} = [100000]_2$

Conversion of fractional decimal number into binary

To convert the fractional decimal number into binary, the fractional number is multiplied by 2. The carry is recorded in the integer position. This procedure is repeated. The carry taken in the forward direction is the binary fraction.

Example 1 : Convert 0.625 into binary number

0.625 x 2 = 1.250 carry 1
0.250 x 2 = 0.50 carry 0
0.50 x 2 = 1.00 carry 1

$[0.625]_{10} = [0.101]_2$

Example 2 : Convert 0.535 into binary number

0.535 x 2 = 1.070 carry 1
0.070 x 2 = 0.14 carry 0
0.14 x 2 = 0.28 carry 0
0.28 x 2 = 0.56 carry 0
0.56 x 2 = 1.12 carry 1

$[0.535]_{10} = [0.10001]_2$

Example 3: Convert 27.6 into binary number

2	27		0.6 x 2 = 1.2	carry	1
2	13	- 1	0.2 x 2 = 0.4	carry	0
2	6	- 1	0.4 x 2 = 0.8	carry	0
2	3	- 0	0.8 x 2 = 1.6	carry	1
	1	- 1	0.6 x 2 = 1.2	carry	1

$[27]_{10} = [11011]_2$ $[0.6]_{10} = [0.10011]_2$

$[27.6]_{10} = [11011.10011]_2$

Conversion of binary into decimal number

To convert the given binary number into a decimal number we have to follow the following steps.

1. First write the binary number.
2. Write the positional value below each digit.
3. Strike the value below the binary number 0.
4. Add the remaining positional value.

It is the desired decimal number.

Example 1:

Convert 11010 into decimal number.

Step 1	:	1	1	0	1	0
Step 2	:	16	8	4	2	1
Step 3	:	16	8	4	2	1
Step 4	:	16 + 8 + 2 = 26				

$[11010]_2 = [26]_{10}$

Example 2 :

Convert 0.1101 into decimal number

Step 1	:	1	1	0	1
Step 2	:	0.5	0.25	0.125	0.0625
Step 3	:	0.5	0.25	0.125	0.0625

Step 4 : 0.5 + 0.25 + 0.0625 = 0.8125

$[0.1101]_2 = [0.8125]_{10}$

Example : 3

Convert 101.01 into decimal number

Step 1	:	1	0	1	0	1
Step 2	:	4	2	1	0.5	0.25
Step 3	:	4	2	1	0.5	0.25

Step 4 : 4 + 1 + 0.25 = 5.25

$[101.01]_2 = [5.25]_{10}$

c. Octal number system

In an octal number system 8 symbols are used. The eight symbols are 0,1,2,3,4,5, 6,7. Hence the base of the system is 8. Therefore the positional value of each digit is the power of eight. The octal number will be 0,1,2,3,4,5,6,7,10,11,12, 13,14,15,6,17,20,21,22,23,24,25,26, 27,30,....

8^3 8^2 8^1 8^0 8^{-1} 8^{-2} 8^{-3}

Conversion of octal number into decimal number

To convert the octal number into decimal number, we have to follow the following steps.

1. First write the octal number.
2. Below each octal digit write the positional value.
3. The multiply the positional value by the corresponding octal digit.
4. In the end odd the product.

The added resulting product is the required decimal number.

Example 1: Convert the octal number 352 into decimal number.

Step 1	:	3	5	2
Step 2	:	8^2	8^1	8^0
Step 3	:	3 x 64	5 x8	2 x 1

Step 4 : 192 + 40 + 2 = 234

$[352]_8 = [234]_{10}$

Example 2: Convert the octal number 23.13 into decimal number.

Step 1	:	2	3	1	3
Step 2	:	8^1	8^0	8^{-1}	8^{-2}
Step 3	:	2x8	3x1	1x(1/8)	3 x (1/64)

Step 4 : 16 + 3 + (1/8) + (3/64) = 19(11/64)

$[23.13]_8 = [19(11/64)]_{10}$

Conversion of decimal number into octal number

To convert the decimal number into octal number, divide the given decimal number repeatedly by 8. The remainder in the reverse order is the octal number.

Example 1 : Convert the decimal number 175 into octal number

8 | 175		
8 | 21	-	7
2	-	5

$[175]_{10} = [257]_8$

Example 2 : Convert the decimal number 99 into octal number

8	99		
2	12	-	3
	1	-	4

$[99]_{10} = [143]_8$

Conversion of fractional decimal number into octal number

To convert the fractional decimal number into octal number, multiply the fractional number by 8. The carry is recorded in the integer positions. The procedure is repeated. The carry taken in the forward direction is the octal fraction.

Example 1 : Convert the fractional decimal number 0.15 into fractional octal number

0.15 x 8 = 1.20	carry 1
0.20 x 8 = 1.60	carry 1
0.60 x 8 = 4.80	carry 4
0.80 x 8 = 6.40	carry 6
0.40 x 8 = 3.20	carry 3
0.20 x 8 = 1.60	carry 1

$[0.15]_{10} = [0.114631]_8$

Example 2 : Convert the decimal number 17.23 into octal number.

8 | 17	0.23 x 8 = 1.84 carry 1
2 - 1	0.84 x 8 = 6.72 carry 6
$[170]_{10} = [21]_8$	0.72 x 8 = 5.76 carry 5
	$[0.23]_{10} = [0.165]_8$

$[17.23]_{10} = [21.165]_8$

Conversion of octal into binary number

The given octal number can be converted into binary using the following table. It gives the relation between octal and binary.

0	1	2	3	4	5	6	7
000	001	010	011	100	101	110	111

1. First write the octal number.
2. Below each octal digit, write the binary equivalent of the octal digit using the above table.
3. Then the binary digits are written in a single group. This is the binary equivalent of the given octal number.

   If we want we can leave a space between group 3 bits.

Example 1 : Convert the octal number 257 into a binary number.

Step 1	:	2	5	7
Step 2	:	010	101	111
Step 3	:	010101111		

$[257]_8 = [010101111]_2$

Example 2 : Convert the octal number 36.24 into a binary number.

Step 1	:	3	6	2	4
Step 2	:	011	110	010	100
Step 3	:	011110.010100			

$[36.24]_8 = [011110.010100]_2$

Example 3 : What is the binary equivalent of decimal number 363 convert to octal, then to binary. Verify your result by direct conversion into binary number.

8	363			
8	45	-	3	$[363]_{10} = [553]_8$
	5	-	5	

5 5 3

101 101 011

$[363]_{10} = [101101011]_2$

2	363		
2	181	-	1
2	90	-	1
2	45	-	0
2	22	-	1
2	11	-	0
2	5	-	1
2	2	-	1
	1	-	0

$[363]_{10} = [101101011]_2$

Hence verified

Conversion of binary number into octal number

The procedure is reverse to that of the conversion of octal into binary number.

1. The given binary number is arranged into groups of 3 bits starting from the octal point.
2. Then convert each group to its equivalent octal number. If necessary add zeroes in the left end.

The final number is the octal number.

Example 1 : Convert the binary number 101001001 into octal number.

Step 1 : 101 001 001

Step 2 : 5 1 1

$[101001001]_2 = [511]_8$

Example 2 : Convert the binary number 10111 into octal number.

Step 1 : 010 111

Step 2 : 2 7

$[10111]_2 = [27]_8$

Example 3 : Convert the binary number 1011.01101 into octal number.

Step 1 : 001 011 011 010

Step 2 : 1 3 3 2

$[1011.01101]_2 = [13.32]_8$

4. Hexadecimal number system

In hexadecimal number system 16 symbols are used. The sixteen symbols are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F. Hence the base of the system is 16. Therefore the positional value of digit is the power of 16. The hexadecimal numbers are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, B, 1C, 1D, 1E, 1F, 20..... The relation between the decimal, binary and hexadecimal is given in the table.

0	0	0000
1	1	0001
2	2	0010
3	3	0011
4	4	0100
5	5	0101
6	6	0110
7	7	0111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111

Conversion of binary number into hexadecimal number

The procedure is reverse to that of the conversion of hexadecimal into binary. The given binary number is arranged into groups of 4 bits starting from the right. Using the table the binary can be converted into hexadecimal digit.

Example 1 : Convert 1011 0101 into hexadecimal number.

1011 0101

B 5

$[1011\ 0101]_2 = [B5]_{16}$

Example 2 : Convert 1011010111 into hexadecimal number.

0010 1101 0111

2 D 7

$[1011010111]_2 = [2D7]_{16}$

Binary arithmetic

i. Binary addition

For binary addition, the following rules should be followed.

1. 0 + 0 = 0
2. 0 + 1 = 1
3. 1 + 0 = 1
4. 1 + 1 = 10

The last rule is often written as 1+ 1 = 0 with a carry of 1.

When adding 1+1+1, first we have to add the first two is

1 + 1 = 10

1 + 1 + 1 = 10 +1

Then we have to add 1 with 10.

10 + 1 = 11

1 + 1 + 1 + 1 = 10 + 1 + 1

= 11 + 1

= 100

When adding a big binary number, first we have to add the digits in the right end column. If there is any carry, it should be added with the next column. This procedure is repeated till the last column.

Example

1. Add 10 and 01

2	1 0	First column 1 + 0 = 1
1	+ 0 1	Second column 0 + 1 = 1
—	———	
3	1 1	
—	———	

2. Add 101 and 110

5	1 0 1	First column 0 + 1 = 1
6	+ 1 1 0	Second column 1 + 0 = 1
—	———	Third column 1 + 1 = 0
11	1 0 1 1	with carry 1 or 1 +1 = 10
—	———	

3. Add 111 and 110

7	1 1 1	First column 0 + 1 = 1
6	+ 1 1 0	Second column 1 +1 = 0 with carry 1
—	———	Third column 1 + 1 + 1 = 10+1 = 11
11	1 0 1 1	
—	———	

Example

1. Find the 2's complement of 0101

   1's complement of 0101 is 1010

   Add 1 with 1's complement

   ```
        1 0 1 0
   ---------
   2's complement   1 0 1 1
   ---------
   ```

2. Find the 2's complement of 11001

   ```
   1's complement   0 0 1 1 0
   2's complement   0 0 1 1 0
                          1
   ---------
                    0 0 1 1 1
   ---------
   ```

c. 1's complement subtraction

For 1's complement subtraction, the following steps should be followed.

1. Find the 1's complement of the number to be subtracted.
2. Add this 1's complement to the number to which the subtraction is required.
3. If there is a carry, add is with the remaining number.
4. If there is an end around carry, the number is positive and it is in binary form.
5. If there is no end – round carry, the answer is negative and it will be in 1's complement. It should be changed into a binary number.

Example

1. Subtract 101 from 111

   1's complement 101 is 010

   ```
     1 1 1
   + 0 1 0
   ---------
   ┌1 0 0 1
   │  0 0 1
   └─────1
   ---------
     0 1 0
   ---------
   ```

2. Subtract 1010 from 1101

   1's complement of 1010 is 0101

   ```
     1 1 0 1
   + 0 1 0 1
   -----------
   ┌1 0 0 1 0
   │  0 0 1 0
   └───────1
   -----------
     0 0 1 1
   -----------
   ```

3. Subtract 1101 from 1010

   1's complement of 1101 is 0010

   ```
     1 0 1 0
   + 0 0 1 0
   ---------
     1 1 0 0
   ---------
   ```

There is no end around carry. So it is a negative number and it will be in 1's complement. So after changing it into a binary number, a negative sign should be attached.

Result – 0011

4. Subtract 01101 from 11011

1's complement of 01101 is 10010

```
  1 1 0 1 1
  1 0 0 1 0
 -----------
1 0 1 1 0 1
  0 1 1 0 1
 -----------
    0 1 1 1 0
 -----------
```

5. Subtract 11011 from 01101

1's complement of 11011 is 00100

```
  0 1 1 0 1
  0 0 1 0 0
 ---------
  1 0 0 0 1
 ---------
```

There is no end around carry. So this number is negative and it is in 1's complementary. So after changing it into a binary number a negative sign should be attached.

Result = –01110

4. 2's complement subtraction

In 2's complement subtraction, the following steps should be followed.

1. First find the 2's complement of the number to be subtracted.
2. Add this complement to the number to which subtraction is required.
3. Drop the carry in the addition.
4. If the carry is 1, the answer is positive and it is in binary form.
5. If there is no carry, re-complement the answer and attach minus sign.

Example :

1. Subtract 101 from 111

2's complement of 101 is 010 + 1 = 011

```
  1 1 1
+ 0 1 1
 -------
1 0 1 0        Ans. : 0 1 0
 -------
Drop
```

2. Subtract 1010 from 1101

2's complement of 1010 is 0101 + 1 = 0110

```
  1 1 0 1
+ 0 1 1 0
 ---------
1 0 0 1 1      Ans. : 0 0 1 1
 ---------
Drop
```

3. Subtract 1101 from 1010

2's complement of 1101 is 0010 +1 = 0011

```
  1 0 1 0
+ 0 0 1 1
---------
  1 1 0 1
---------
```

No carry

There is no carry. So we have to recomplement the answer.

1101 – 1 = 1100 = 0011

Final answer is = 0011

iii. Binary multiplication

For binary multiplication, we have to follow the following rules.

1. 0 x 0 = 0
2. 0 x 1 = 0
3. 1 x 0 = 0
4. 1 x 1 = 1

Example

1. Multiply 111 by 101

```
      111
  x   101
----------
      111
     000
    111
----------
  100011
----------
```


2. Multiply 1101 by 1100

```
      1 1 0 1
  X   1 1 0 0
-------------
    0 0 0 0
  0 0 0 0
1 1 0 1
1 1 0 1
-------------
1 0 0 1 1 1 0 0
-------------
```

3. Multiply 10110 by 101

```
      1 0 1 1 0
  X       1 0 1
-------------
      1 0 1 1 0
    0 0 0 0 0
  1 0 1 1 0
-------------
  1 1 0 1 1 1 0
-------------
```

iv. Binary division

For binary division, we have to follow the following rules.

1. 0 ÷ 1 = 0 or 0/1 = 0
2. 1 ÷ 1 = 1 or 1/1/ = 1

Example

1. Divide 1100 by 10

```
    110
   ----
10) 1100
    10
   ----
     10
     10
   ----
      00
   ----
```

Ans. : 110

2. Divide 11001 by 101

```
     101
   -------
101) 11001
     101
   -------
      101
      101
   -------
```

Ans. : 101

Binary codes

There are several methods that are used to express both numbers and letters as binary codes. These methods are discussed below.

The 8421 code

The 8421 code expresses each decimal digit 0 through 9, by its 4-bit binary equivalent. For example, the decimal number 439 is changed to its binary equivalent as given below.

4	3	9
0100	0011	1001

Similarly, in the 8421 code, 010000101001 stand for the decimal number 429. To cite another example, let us take 8963 for encoding to 8421 code.

8	9	6	3
1000	1001	0110	0011

Table : The 8421 code and binary equivalents of some decimal numbers.

Decimal	8421 code			Binary
0			0000	0000
1			0001	0001
2			0010	0010
3			0011	0011
4			0100	0100
5			0101	0101
6			0110	0110
7			0111	0111
8			1000	1000
9			1001	1001
10		0001	0000	1010
11		0001	0001	1011
12		0001	0010	1100
13		0001	0011	1101
98		1001	1000	1100010
99		1001	1001	1100011
100	0001	0000	0000	1100100
101	0001	0000	0001	1100101
102	0001	0000	0010	1100110
578	0101	0111	1000	1001000010

Table shows some more conversion of decimal numbers to the 8421 code. The largest 4-bit group in the 8421 code is 1001. In other words, only 10 of the 16 possible 4-bit groups are used. The 8421 code does not use the numbers 1010, 1011, 1100, 1110, 1111.

The 8421 code is identical to binary equivalents of decimal numbers 0 through 9. Because of this it is called the 8421 code, the weights in the groups are 8, 4, 2, 1, reading from left to right i.e., the same as for binary numbers.

In may be observed from table that the 8421 code, above decimal 9, differs from the binary-number code. For example, the binary number for 12 is 1100, but the 8421 number for 12 is 0001 0010. The decimal number 24 is 11000 in binary, but it becomes 0010 0100 in the 8421 code. Therefore, above decimal 9, every binary number differs from the corresponding 8421 number.

Advantages and disadvantages

The main advantage of the 8421 code is the ease in converting to and from decimal numbers, we need only to remember the binary numbers for 0 through 9 because we encode in 8421 code only one decimal digit at a time. A disadvantage, however, of the 8421 code is that, the rules for binary additions do not apply to the entire 8421 number, but only to the individual 4bit groups. For instance, adding 12 and 9 is easier in straight binary, than in the 8421 code.

12	1100
+9	+1001
---	------
21	10101 → 21
---	------

In the 8421 code, we get an unacceptable answer.

12	00010010
+9	+1001
---	----------
21	00011011(?)
---	----------

We are unable to decode 0001 1011 in 8421 code because 1011 does not exist in the 8421 code. Therefore, the additional of 8421 numbers is not as simple as for binary numbers.

BCD codes

The 8421 code is one of the many codes referred to as Binary Coded Decimal (BCD) code. In general, a BCD code is one in which the digit of a decimal number are encoded one at a time, into groups of binary digits. For this encoding, we can use 4-bit groups, 5-bit groups, 6-bit groups, etc. The 8421 code is a mixed base code it is binary within each group of 4 bits, but decimal from group to group.

The 8421 code, as discussed earlier, is the most natural type of BCD code. Therefore, it is often referred to as BCD, without qualifying it as 8421. It is called natural because each 4 bit binary group is coded as a decimal equivalent of a number between 0 and 9. A few more examples of conversion of decimal numbers into BCD numbers are given below.

4	4	5			
	0100	0101			
b.	7	3	2		
	0111	0011	0010		
c.	9	4	6	8	5
	1001	0100	0110	1000	0101

Note that each group of four binary bits, as used here, is positionally weighted, from left-to-right as 8421 for conversion to its equivalent decimal number. The 8421 code is, therefore, a positionally weighted binary code used to convert decimal numbers.

The excess-3 code

The excess-3 code (abbreviated XS3) is not a positionally weighted BCD code. It is therefore a non-weighted code, used

to express decimal numbers. To encode a decimal number into its excess-3 form, we as the name implies, add 3 to each decimal digit before converting it to binary. For example, to convert 14 to an excess -3 number, we proceed as follows.

```
 1  4
+3 +3     (Add 3 to each decimal digit)
-----
 4  7     (Resulting decimal digits)
-----
```

We have added 3 to each decimal digit of the decimal number 14. Now we convert each resulting decimal digit to its 8421 binary equivalent. That is,

```
 4    7
0100  0111   (Excess-3 code for decimal 14)
```

So, 0100 0111 in the excess-3 code stands for decimal 14.

As another example, let us convert the decimal number 29 o its excess-3 number.

```
 2      9     (Decimal number)
+3     + 3    (Add 3 to each decimal digit)
-----  ----
 5      12    (Resulting decimal digits)
-----  ----
0101   1100   (Excess-3 code for decimal 29)
```

Note that after adding 9 and 3, we have not carried the 1 to the next column, instead, we left the result intact as 12, then converted as shown. Therefore, 0101 1100in the excess-3 code stands for decimal 29.

Excess-3 addition

Case 1

In excess-3 code, whenever we add two decimal digits, whose sum is 9 or less, an excess-6 number results. To return to excess-3 form, we must subtract 3. For instance, let us add 2 and 5 in excess-3 code.

```
 2      0101      (Excess-3 equivalent of 2)
+ 5    + 1000     (Excess-3 equivalent of 5)
-----  -------
 7      1101      (Excess -6 equivalent of 7)
      -  0011     (subtract 3(0011))
       -------
       1010  (Excess-3 equivalent of 7)
       -------
```

We added two excess-3 numbers and got an excess-6 number. To restore the answer to excess-3 form, we subtracted (0011) from the excess-6 number. The final answer is 1010, which is the excess-3 equivalent of 7.

As another example, let us add 43 and 36 in excess-3 code.

```
 43     0111 0110   (Excess-3 equivalent of 43)
+ 36   + 0110 1001  (Excess-3 equivalent of 36)
-----  ----------
 79     1101 1111   (Excess -6 equivalent of 79)
      - 0011 0011  (subtract 3(0011) from each group)
        ----------
        1010 1100  (Excess-3 for decimal 79)
        ----------
```

In the above example, there was no carry in either group. So the decimal sum was 9 or less for each group. As a result,

the answer was in excess-6 form and we subtracted 3(0011) from each group to return to excess-3 code.

Case 2

Whenever the sum of decimal digits exceeds 9, there will be a carry from one group to the next. When this happens, the group that produces the carry will revert to 8421 form this occurs because of the excess-6 and the six unused four-bit groups. To restore the answer to the excess-3 code, we must add 3 (0011) to the group that produces the carry. For instance, to add 29 and 39, we proceed as follows.

		Column A		Column B	
	29	0101		1100	(Excess – 3 of 29)
+	39	0110		1100	(Excess – 3 of 39)
					(Observe the carry
	68	1011	1000		obtained from column B carry
		+ 1			is added to column A)
		1100	1000		(The first result)
		– 0011	+ 0011		(Subtract 0011 and add 0011 as
					shown)
		1001	1011		(Excess-3 of decimal 68)

In column B we added 1100 to 1100, to get 1000, with a carry of 1 into column A. In column A, we added 0101, 0110 and the carry, to get 1100 with no carry. The first result in column B is back to 8421 form because this column produced a carry. The first result in column A is still in excess-6 form because this column does not produce a carry. Therefore, we must subtract 0011 from column A and add 0011 to column B. The final answer is 1001 1011, the excess-3 number for decimal 68.

Let us now summarize the addition rules with excess-3 numbers.

1. Add the exces-3 numbers using the rules for binary addition.
2. If any group produces a decimal carry, add 0011 to that group.
3. If any group does not produce a decimal carry, subtract 0011 from that group.

The excess – 3 code has the advantage that all operations in addition can be performed using the rules of ordinary binary addition. The 8421 code, on the other hand, requires special operations to handle decimal carries. Also, the excess-3 code has the advantage that the 1's or the 2's complements can be used to subtract excess-3 numbers.

The exce-3 cod is also called Xs3.

Let us solve a few more examples to illustrate the rules of BCD codes discussed so far.

3. Express the decimal numbers 328 and 1497 in 8421 BCD code

3	2	8
0011	0010	1000

$(328)_{10}$ = 0011 0010 1000 in BCD code.

1	4	9	7
0001	0100	1001	0111

$(1497)_{10}$ = 0001 0100 1001 0111 in BCD code.

b. Express the decimal number 124 and 7621 inXS3.

i.

	1	2	4
+	3	3	3
	4	5	7
	0100	0101	0111

$(124)_{10}$ = 0100 0101 0111 in XS3 code.

ii.

	7	6	2	1
+	3	3	3	3
	10	9	5	4
	1010	1001	0101	0100

$(7621)_{10}$ = 1010 1001 0101 0100 is XS3 code.

c. Add the XS3 numbers 0011 and 0100 and then 0110 and 1010. Express the result in XS3 code.

i.

	0011	XS3
+	0100	XS3
	0111	XS6 sum
–	0011	Subtract 0011 from the XS6 sum
	0100	XS3 of sum of 0011 and 0100

ii.

	0110	XS3
+	1010	XS3
	10000	XS6 sum with a carry
	0011	Add 0011 to the result
	0011	XS3 sum of 0110 and 1010

d. Find the XS3 sum of (i) 29 and 39 and (ii) 43 and 36.

i.

	29	0101 1100	(XS3 of decimal 29)
+	39	+ 0110 1100	(XS3 of decimal 39)
	68	+ 1011 1000	
		1	
		1100 1000	
		– 0011 0011	
		1001 10011	XS3 of decimal 68

ii.

	43	0111 0110	XS3 of decimal 43
+	36	0110 1001	XS3 of decimal 36
	79	1101 1111	XS6 of decimal 79
		–0011 –0011	subtract 0011
		1010 1100	XS3 of decimal 79

The Gray Code

The Gray code is an unweighted code not suited for arithmetic operations, but useful for input/output devices, analog to digital converters, and other peripheral equipment.

Table shows the gray code, along with the corresponding binary numbers. Each gray number differs from the preceding number in only one digit position. For example, in going from decimal 8 to 9, The gray code numbers change from 1100 to 1101, these numbers differ only in the least significant bit To cite another example, the decimal numbers 13 and 14 are represented by gray-code numbers 1011 and 1001, these

numbers differ in only one digit position namely the second position from the right.

Table : Gray code

Decimal	*Gray code*	*binary*
0	0000	0000
1	0001	0001
2	0011	0010
3	0010	0011
4	0110	0100
5	0111	0101
6	0101	0110
7	0100	0111
8	1100	1000
9	1101	1001
10	1111	1010
11	1110	1011
12	1010	1100
13	1011	1101
14	1001	1110
15	1000	1111

We thus see that only one bit in the gray code number changes each time the decimal number is incremented i.e, the gray code requires only one bit to change when we increment a decimal number.

Binary to gray conversion

The first (i.e. the most significant) gray digit is the same as the first binary digit. We then add each pair of adjacent

binary bits to get the next gray digit. The carries, if any are disregarded.

This form of addition is formally called the mode-2 addition or exclusive OR addition. The four rules for this kind of addition are :

$$0 + 0 = 0$$
$$0 + 1 = 1$$
$$1 + 0 = 1$$
$$1 + 1 = 0$$

Let us take an example and convert the binary number 1100 to its gray code equivalent.

Step 1 : The first gray digit is the same as the first binary digit. So, we repeat the first digit as illustrated below.

1 1 0 0 Binary

↓

1 Gray

Step 2 : Now, we add the first 2 bits of the binary number using the rules of mode-2 addition. The carry, if any, is disregarded.

The sum is the next gray digit as shown below

1 1 1 0 0 binary

↓

1 0 Gray

Step 3: Add the next two binary digits to get the next gray digit.

```
1 1 → 0 0  binary
      ↓
1 0   1    Gray
```

Step 4 : Add the last two binary digits to get the gray digit.

```
1 1 0 → 0  binary
        ↓
1 0 1   0  Gray
```

Therefore, 1010 is the gray-code equivalent of the binary number 1100.

The above procedure can be shortened as follows : Wherein the conversion is shown to have been performed in a single step.

```
1 → 1 → 0 → 0  Binary
↓   ↓   ↓   ↓
1   0   1   0  Gray
```

Similarly, to convert the binary number 110100110 to Gray code, we can write as follows ;

```
1 → 1 → 0 → 1 → 0 → 0 → 1 → 1 → 0  Binary
↓   ↓   ↓   ↓   ↓   ↓   ↓   ↓   ↓
1   0   1   1   1   0   1   0   1  Gray
```


The conversion of the binary number 1000110111to gray number is also shown below.

```
1 → 0 → 0 → 0 → 1 → 1 → 0 → 1 → 1 → 1   Binary
↓   ↓   ↓   ↓   ↓   ↓   ↓   ↓   ↓   ↓
1   1   0   0   1   0   1   1   0   0   Gray
```

Gray – to – binary conversion

To convert from gray code back to binary, we use a method that is similar to binary-to-gray code conversion but not exactly the same. Again, an example will best describe the method. Let us convert the gray code number 101110101 back to its binary equivalent.

Step 1 : Repeat the most significant digit.

```
1 → 0  1 → 1 → 1 → 0 → 1 → 0 → 1   Gray
↓
1                                   Binary
```

Step 2 : Add diagonally as shown to get the next binary digit

```
1 0 1 1 1 0 1 0 1   Gray
  ↗
1 1                 Binary
(1 + 0 = 1)
```

Step 3 : Continue adding diagonally to get the remaining binary digits.

```
1 0 1 1 1 0 1 0 1   Code
  ↗ ↗
1 1 0 1 0 0 1 1 0   Binary
```

Weighted binary codes

Many systems of codes are used to express the decimal digits, 0 through 9. We learnt one such weighted code, i.e., 8421. Similarly, there are other weighted codes such as 2421, 5211 and so forth. Each four-bit group represents one decimal digit. To recapitulate for instance let us convert the number 763_{10} to 8421 code.

7	6	3
↓	↓	
0111	0110	0011

In the 8421 code, the weights of binary bits in each four-bit group are 8, 4, 2, 1 starting from left and going on right. Thus, this is how the four-bit group 0111 converts to decimal 7.

Binary :	0	1	1	1
Positional weights :	8	4	2	1

Decimal : 0 + 4 + 2 + 1 = 7

It the same binary group 0111 were to be in 2421 code, the conversion to decimal can be obtained as follows :

Binary :	0	1	1	1
Positional weights :	2	4	2	1

Decimal : 0 + 4 + 2 + 1 = 7

Now study table wherein three weighted codes are used to express decimal digits 0 through 9.

Table : Weighted binary codes

Decimal	8421	2421	5211
0	0000	0000	0000
1	0001	0001	0001
2	0010	0010	0011
3	0011	0011	0101
4	0100	0100	0111
5	0101	1011	1000
6	0110	1100	1010
7	0111	1101	1100
8	1000	1110	1110
9	1001	1111	1111

Another weighted code is 5043210. This biquinary code is an example of a seven-bit code with error-detection properties. Each biquinary code consists of five 0s and 1s placed in the corresponding weighted columns. One or more bits may change [illegible]. The biquinary codes of the decimal digits 0 through 9 are given in table.

Table : Binary Code

Decimal	Biquinary 5043210
1	0100001
2	0100010
3	0100100
4	0101000
5	0110000
6	1000010
7	1000100
8	1001000
9	1010000

ASCII code

The American Standard Code for Information Interchange (abbreviated ASCII, pronounced 'as kee') is widely used for printers, keyboards and video terminals that interface with small computer systems. ASCII is an alphanumeric code for letters, numbers and other symbols.

ASCII is basically as seven bit code. Its format is $X_6\ X_5\ X_4 X_3 X_2 X_1 X_0$. Each X is a 0 or a 1. For example, the capital letter 'D' is encoded as 1000100. The lower case letter 'd' is encoded as 1100100. Hitting the key D or d on the keyboard will send the corresponding code into the computer. Similarly, the digits 0 through 9 and several punctuation and mathematical symbols can be encoded in the ASCII code. An eighth bit is usually added and is used as a parity bit. The addition of a parity bit produces an 8-bit number in the format $X_6 X_5 X_4 X_3 X_2 X_1 X_0$. Where X_7 is the parity bit. The use of the parity bit is explained in section.

Solved Examples

1. Convert the following decimal number to their equivalent binary numbers.

a. $(24)_{10}$

Sucessive division		Remainder
2	24	0
2	12	0
2	6	0
2	3	1
2	1	1
	0	

$(24)_{10} = (11000)_2$

b. $(7)_{10}$

Sucessive division		Remainder
2	7	1
2	3	1
2	1	1
	0	

$(7)_{10} = (111)_2$

c. $(72)_{10}$

Sucessive division		Remainder
2	72	0
2	36	0
2	18	0
2	9	1
2	4	0
2	2	1
2	1	1
	0	

$(72)_{10} = (1001000)_2$

d. $(237)_{10}$

Sucessive division		Remainder
2	237	1
2	118	0
2	59	1
2	29	1
2	14	0
2	7	1
2	3	1
2	1	1
	0	

$(237)_{10} = (11101101)_2$

e. $(824)_{10}$

Sucessive division		Remainder
2	824	0
	412	0
	206	0
	103	1
	51	1
	25	1
	12	0
	6	0
	3	1
	1	1
	0	

$(824)_{10} = (1100111000)_2$

Examples

Convert the following binary numbers to gray code.

Solution

a. $(1111)_2$

$1 \rightarrow 1 \rightarrow 1 \rightarrow 1$ Binary

$\downarrow \quad \downarrow \quad \downarrow \quad \downarrow$

$1 \quad 0 \quad 0 \quad 0$ Gray

$(1111)_2 = 1000$ in Gray

b. $(101011)_2$

$1 \rightarrow 0 \rightarrow 1 \rightarrow 0 \rightarrow 1 \rightarrow 1$ Binary

$\downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow$

$1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 0$ Gray

$(101011)_2 = 111110$ in Gray

c. $(1110)_2$

$1 \rightarrow 1 \rightarrow 1 \rightarrow 0$ Binary

$\downarrow \quad \downarrow \quad \downarrow \quad \downarrow$

$1 \quad 0 \quad 0 \quad 0$ Gray

$(1110)_2 = 1001$ in Gray

d. $(10110)_2$

$1 \rightarrow 0 \rightarrow 1 \rightarrow 1 \rightarrow 0$ Binary

$\downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow$

$1 \quad 1 \quad 1 \quad 0 \quad 1$ Gray

$(10110)_2 = 11101$ in Gray

Convert the following Gray code numbers to binary numbers

Solution

a. 10111 in gray

$1 \quad 0 \quad 1 \quad 1 \quad 1 \quad 1$ Gray

$\downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow$

$1 \quad 0 \quad 0 \quad 1 \quad 0 \quad 1$ Binary

10111 in gray $= (1100101)_2$

b. 10101010 in gray

$1 \quad 0 \quad 1 \quad 0 \quad 1 \quad 0 \quad 1 \quad 0$ Gray

$\downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow$

$1 \quad 1 \quad 0 \quad 0 \quad 1 \quad 1 \quad 0 \quad 1$ Binary

10101010 in gray $= (11001100)_2$

c. 101010 in gray

$1 \quad 0 \quad 1 \quad 0 \quad 1 \quad 0$ Gray

$\downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow$

$1 \quad 1 \quad 0 \quad 0 \quad 1 \quad 0$ Binary

101010 in gray $= (110010)_2$

d. 1110101 in gray

1	1	1	0	1	0	1	Gray
1	0	1	1	0	0	1	Binary

1110101 in gray = $(1011001)_2$

e. 110110101 in gray

1	1	0	1	1	0	1	0	1	Gray
1	0	0	1	0	0	1	1	0	Binary

110110101 in gray = $(100100110)_2$

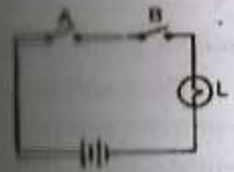
Basic logic gates

In amplifiers, the transistor is operated as a linear current and voltage amplifier. In this the output change according to the change in input. In some other circuits semiconductor device is used to operate as ON and OFF switch. The action of such circuits are non-linear and operated to give ON and OFF switch action. A switch that can be opened or closed is known as the gate. Thus a gate circuit has two possible sates. These states can be described as ON or OFF, true or false, yes or no. Mathematically the two states are represented by the numbers 1 and 0. Thus I may represent the closed switch and 0 may represented the open switch.

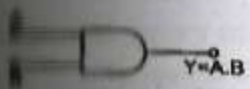
The circuits which perform the switching action are known as logic circuit or logic gates. A logic gate my have a number possible inputs. The output signal will be obtained only if the input signal meets specific conditions. Different conditions for input signal give different types of logic gates. The basic three logic gates are 1. AND gate, 2. OR gate, 3. NOT gate.

The AND gate

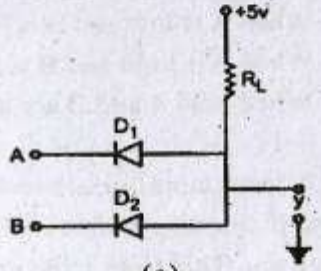
The AND gate is sometimes called as all or nothing gate. The operation of an AND gate can be explained using the circuit shown in figure (a).



(a)



(b)



(c)

The switches A and B are connected in series with a lamp L and a cell. When the two switches A and B are closed, then only lamp L will give light. If any one of the switch is not closed, the lamp will not give light. Thus when all the switches are closed, then only three will be an output. Thus the electrical circuit is equivalent to AND gate. Mathematically it can be written as

$$A \bullet B = L$$

Thus in an AND gate the output will be high only if all the inputs are high. If any one of the input is low, the output will be low.

A	B	Y = A . B
0	0	0
0	1	0
1	0	0
1	1	1

In circuits the AND gates are represented by the symbols as shown in figure (b). Here A and B are the inputs and y is the output.

There are four different cases.

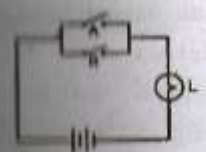
1. When both A and B are low, the output y will be low.
2. When A is low and B is high, the output y will be low.
3. When A is high and B is low, the output y will be low.
4. When both A and B are high, the output y will be high.

A truth table for a two input AND gate is shown in the table. In this all possible inputs and the corresponding outputs are given. This truth table explains the operation of an AND gate. The high level is represented by 1 and the low level is by 0.

A diode implementation of a positive two input AND gate is shown in figure(c). In the diode circuit, if there is no input at each diode, the two diodes are forward biased and the output will be zero. If A = 5 volts (1 state) B = 0 volt, the D_1 would not conduct and D_2 will conduct. The output will remains at zero level. If A = B = 5 volts, the two diodes are reverse biased. So the output will rise to 5 volts (1 state). Hence an output will result only when A and B are present. Thus this circuit functions as an AND gate. We can form AND gate with more inputs.

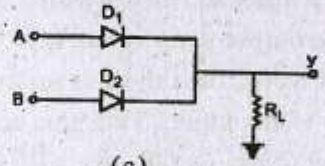
b. The OR gate

The OR gate is sometimes called as any or all gate. The operation of an OR gate can be explained using the circuit shown in figure(a).



(a)

(b)



(c)

Two switches A and B are connected in parallel. The parallel switch is connected across a lamp L and a cell. When the switch A or switch B or both is closed, the lamp L will give light. When the two switches are not closed, the lamp will not give light. Thus the electrical arrangement is equivalent to OR gate. Mathematically it can be written as A + B = L.

Thus in an OR gate the output will be high, if any on of the input is high. The output will low when all the inputs are low. In circuits the OR gate is represented by symbol as shown in figure (b). Here A and B are the inputs and y is the output.

There are four different cases.

1. When both A and B are low, the output y will be low.
2. When A is low and B is high, the output y will be high.
3. When A is high and B is low, the output y will be high.
4. When both A and B are high the output y will high.

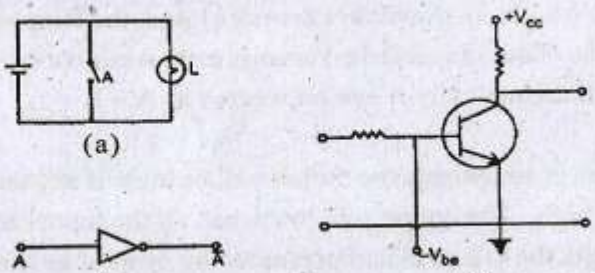
A truth table for a two input OR gate is shown in the table. The truth table explains all the possible operations of an OR gate. If any one of the inputs is high, the output will be high.

A	B	Y = A + B
0	0	0
0	1	1
1	0	1
1	1	1

Figure (c) shown the diode OR gate consisting of two ideal diodes D_1 and D_2 connected in parallel across the output y. If A = 5 volts and B = 0 volts, the diode D_1 will conduct and hence output y = 5 volts. If A = 0 volts and B =5 volts, If A = B = 0 volts, then there is no output. If A = B = 5 volts then there is an output. Thus this circuit functions as an OR gate. We can form on OR gate with more inputs.

c. The NOT gate

It is so called because its output is not the same as its input. It is also called an inverter because it inverts the input signal. It has one input and one output.



The operation of a NOT gate can be explained using the circuit shown in figure (a). When the switch A is closed (that is logic input is in 1 state), the bulb does not glow. (output is in 0 state) because the closed switch short circuits the bulb. Similarly when the switch is open (logic input is in 0 state), the bulb glows (output is in 1 state). Thus it explains the inversion of input.

In circuits the NOT gate is represented by the symbol shown in figure (b). Here A is the input and $y = \overline{A}$ is the output.

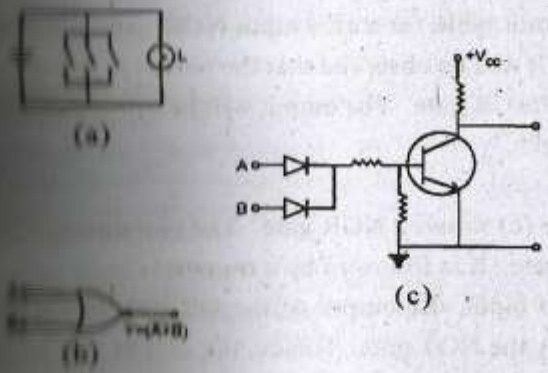
If the input A = 0, then the output y = 1. If the input A = 1, then the output y = 0. It is shown in the truth table.

A	$Y = \overline{A}$
0	1
1	0

Figure (c) is a simple amplifier circuit so that output is out of phase to input. In the absence of any signal, there is no collector current because transistor is biased beyond the cutoff. Hence the output reaches the full supply voltage. When a positive voltage is applied at the input transistor conducts so that collector potential drops to low voltage level due to saturation. Now there is no output. Thus the circuit functions as a NOT gate.

d. The NOR gate

When an OR gate is combined with a NOT gate is cascade, the resultant gate is called NOR gate.



The operation of a NOR gate can be explained using the circuit shown in figure (a). The switches are connected in parallel. The lamp and the cell are connected as shown in figure. If anyone of the switches is in state 1 i.e., closed, the lamp will not glow. (0 state) ie If they are open, then the lamp

will glow. Thus the electrical arrangement is equivalent to a NOR gate. Mathematically it can be written as $L = \overline{A + B}$.

Thus in a NOR gate the output will be high only if all the inputs are low. If any one of the input is high, the output will be low.

A	B	$Y = \overline{A + B}$
0	0	1
0	1	0
1	0	0
1	1	0

In circuits the NOR gate is represented by the symbol shown in figure (b). The bubble is in the end indicates the inversion of the output.

There are four different cases

1. When both A and B are low, the output y will be high.
2. When A is low and B is high the output y will be low.
3. When A is high and B is low the output y will be low.
4. When both A and B are high, the output y will be high.

The truth table for a two input NOR gate is as shown in the table. It will be observed that the output is just the reverse of that of the OR gate. The output will be low if any one of the input is high.

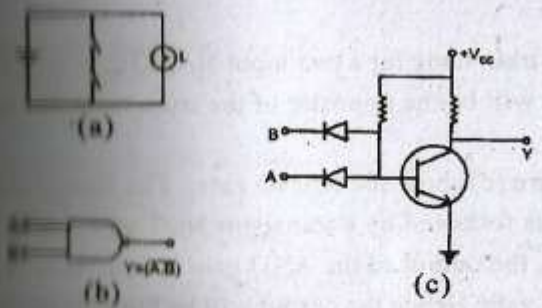
Figure (c) shows a NOR gate. The two diodes in parallel is an OR gate. It is followed by a transistor NOT gate. When there is no input, the output of the OR gate is low. This is inverted by the NOT gate. Hence, the output will be high.

If any one of the input is high or both the inputs are high, the output of the OR gate will be high. This is inverted by the NOT gate. Hence, the output will be low. Thus this circuit functions as a NOR gate.

A NOR gate can be used to realize the basic logic functions such as OR, AND and NOT. A NOR gate followed by a NOT gate will function as an OR gate. If NOT gate are connected to the input, then it will function as an AND gate. If the inputs are connected together, it will function as a NOT gate.

The NAND gate

When an AND gate is combined with a NOT gate is formed, the resultant gate is NAND gate.



The operation of a NAND gate can be explained using the circuit shown in figure (a). the two switches are connected in series. The lamp and the cell are connected as shown in figure. If the switches A and B are closed, the lamp will not glow. Thus if the both the inputs A and B are high the output will be low. When any one of the switches is open the output will be high.

Thus in a NAND gate the output will be low if all the inputs are high. If any one of the input is low, the output will be high.

In circuits the NAND gate is represented by the symbol as shown in figure (b). The bubble indicates the inversion of the output.

There are four different cases.

1. When both A and B are low, the output will be high.
2. When A is low and B is high, the output will be high.
3. When A is high and B is low, the output will be high.
4. When A and B are high, the output will be low.

A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

The truth table for a two input NAND gate is shown in the table. It will be the opposite of the truth table for AND gate.

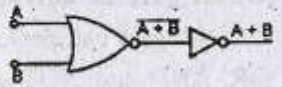
Figure (c) show the NAND gate. The diodes act as AND gate. It is followed by a transistor NOT gate. When there is no input, the output of the AND gate is low. It is inverted by the NOT gate. Hence the output will be high. If any one of the inputs is low, the output of the AND gate is low. It is inverted by the NOT gate. Hence the output will be high. If both the inputs are high, the output of the AND gate is high. It is inverted by the NOT gate. So the output will be low. Thus this circuit functions as a NAND gate. The NAND gate is also called universal gate because it can perform all the three logic functions of an OR, AND and NOT gates.

f. NOR as universal gate

A NOR gate can be used to realize the basic logic functions such as OR, AND and NOT. A NOR gate followed by a NOT gate followed by a NOT gate will function as an OR gate. If a NOT gate is connected in the input, then it will function as an AND gate. If the inputs are connected together, it will function as a NOT gate.

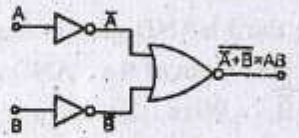
i. as OR gate

The inputs of the NOR gate are A and B. the output from the NOR gate is $\overline{A + B}$. This is given as input to the NOT gate. The final output is inverted and it is given by $\overline{\overline{A + B}}$. This is the logic function of normal OR gate.



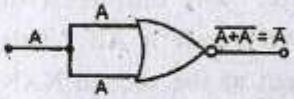
ii. as AND gate

Two NOT gates are connected to the two inputs of the NOR gate. A and B are the inputs for the two NOT gate. The out of the NOT gate are $\overline{A}$ and $\overline{B}$. These are given as input to the NOR gates. The output of the NOR gate is $\overline{\overline{A} + \overline{B}}$. According to Demorgans theorem it is equal to AB. Which is the logic function of normal AND gate.



iii. as NOT gate

Here the two inputs are tied together the output of the NOR gate is $\overline{A + A}$. With the help of Demorgans theorem. It can be proved to be equal to $\overline{A}$. This is the logical function of a normal NOT gate.



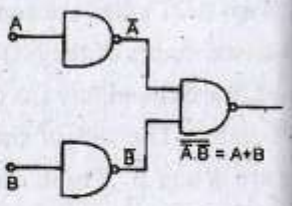
Thus a NOR gate functions as OR, AND and NOT gates. So NOR gate is called as universal gate.

g. NAND gate as universal gate

NAND gate can perform all the three logic functions of an OR, AND and NOT gates. So the NAND gate is also called as universal gate.

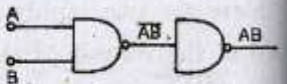
i. as OR gate

The OR gate function can be obtained using three NAND gates. Two NAND gates are connected in the input. Hence the input of the third NAND gate is $\overline{A}$ and $\overline{B}$. So the output of the NAND gate is $\overline{A} \bullet \overline{B}$. With the help of the Demorgans theorem, it can be proved to be equal to A+B. This is the logical function of a OR gate.



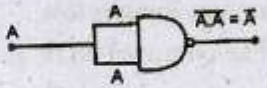
ii. as AND gate

Using two NAND gates, AND function can be performed. A and B are the inputs of the first NAND gate. The output of the first NAND gate is $\overline{AB}$. This is the input of the second NAND gate and hence the output of this is AB which is the function of an AND gate.



iii. as NOT gate

Here the two inputs are tied together. The output of the NAND gate is $\overline{A}\,\overline{A}$ which is equal to $\overline{A}$. This functions as a NOT gate.



Five Mark questions

1. For positional value, the binary system uses the powers of
   a. 2 b. 8 c. 10 d. 16
2. The decimal equivalent of the binary number 1111 is
   a. 10 b. 15 c. 17 d. 28
3. Which of the following is not an octal number
   a. 18 b. 77 c. 222 d. 101
4. The base of hexadecimal number is
   a. 2 b. 8 c. 16 d. 10
5. The hexadecimal equivalent of binary number 1010 is
   a. 9 b. 8 c. A d. 12
6. The decimal equivalent of the hexadecimal number B is
   a. 8 b. 16 c. 12 d. 11
7. Logic circuits perform
   a. amplification b. oscillation
   c. modulation action d. switching action
8. The gate which is called as all or nothing gate is
   a. OR gate b. NOT gate
   c. NAND gate d. AND gate
9. In the AND gate the output will be high
   a. only when all inputs are low
   b. only when all inputs high
   c. only one of the input is low
   d. always

UNIT - IV
BOOLEAN ALGEBRA, ARITHMETIC AND COMBINATIONAL LOGIC CIRCUITS

Boolean Algebra

Boolean algebra is different from ordinary algebra and t
binary. This algebra was developed by Boole in 1854. In Boole
algebra 1+1 = 1. But in binary 1 +1 = 10. Even though the Boole
algebra is in nature like binary, but it is entirely different.

Boolean algebra permits only two values or states fo
variable. The two permitted states of Boolean algebra are usua
represented by 0 and 1. Only three operations are employed
variable in Boolean algebra. They are

1. OR addition represented by plus (+) sing
2. The AND multiplication represented by a (x) or a dot (•
3. The NOT operation represented by a bar over the variab

These operations are different from ordinary algebra.
this algebra there is no fraction and also no negative number.

a. Laws of Boolean algebra

Boolean algebra is a system of Mathematics based on log
It has its own set of fundamental laws. Some laws are just li
ordinary algebraic law. But most of the laws are different.

1. Commutative law

$A + B = B + A$ ... (1)

$A \cdot B = B \cdot A$ ...(2)

2. Associative Law

$A + (B + C) = (A + B) + C$ ... (3)

$(A + B) + (C + D) = A + B + C + D$ ... (4)

$A \cdot (B \cdot C) = (A \cdot B) \cdot C$ ... (5)

3. Distributive Law

$A (B + C) = AB + BC$ ... (6)

$A + BC = (A + B) (A + C)$ ... (7)

$A + \bar{A}B = A + B$ ... (8)

4. OR Law

$A + 0 = A$ ... (9)

If $A = 0$, then $0 + 0 = 0$

If $A = 1$, then $1 + 0 = 1$

$A + A = A$ ... (10)

If $A = 1$, then $1 + 1 = 1$

If $A = 0$, then $0 + 0 = 0$

$A + 1 = 1$ ... (11)

If $A = 0$, then $0 + 1 = 1$

If $A = 1$, then $1 + 1 = 1$

$A + \bar{A} = 1$ ... (12)

If $A = 0$, then, $\bar{A} = 1$, $0 + 1 = 1$

If $A = 1$, then, $\bar{A} = 0$, $1 + 0 = 1$

5. AND Law

$A \cdot 1 = A$ ... (13)

If $A = 0$, then $0 \cdot 1 = 0$

If $A = 1$, then $1 \cdot 1 = 1$

$A \cdot 0 = 0$ ... (14)

If $A = 0$, then $0 \cdot 0 = 0$

If $A = 1$, then $1 \cdot 0 = 0$

$A \cdot \bar{A} = A$ ... (15)

If A = 0 then 0.0 = 0

If A = 1, then 1.1 = 1

$$A \cdot \overline{A} = 0 \qquad \ldots (16)$$

If A = 0, then $0.\overline{0} = 0.1 = 0$

If A = 1, then $1.\overline{1} = 1.0 = 0$

Example 1 :

Prove that A + AB = A

Case 1 : A = 0, B = 0

A + AB = A

0 + 0.0 = 0

0 + 0 = 0

0 = 0

Case 2: A = 0, B = 1

A + AB = A

0 + 0.1 = 0

0 + 0 = 0

0 = 0

Case 3 : A = 1, B = 0

A + A.B = A

1 + 1.0 = 1

1 + 0 = 1

1 = 1

Case 4: A = 1, B = 1

A + A.B = A

1 + 1.1 = 1

1 + 1 = 1

1 = 1

Thus A + AB = A is checked for all possible values.

Example 2:

Prove the Boolean identity AC + ABC = AC

Solution :

L.H.S = AC + ABC = AC (1 + B)

1 + B = 1

∴ L.H.S = AC.1 = AC = R.H.S

∴ AC + ABC = AC

Example 3:

Prove that (A + B) (A + C) = A + AC

Solution :

L.H.S = (A + B) (A + C)

= AA + AC + AB + BC

= A + AC + AB + BC (∴ A.A = A)

= A + AB + AC + BC

= A (1 + B) + AC + BC

= A + AC + BC (∴ 1 + B = 1)

= A (1 + C) + BC (∴ 1 + C = 1)

= A + BC

(A + B) (A + C) = A + BC

Example 4 :

Simplify the Boolean Expression

$A B \overline{C} + A \overline{B} C + \overline{A} B C + A B C + A \overline{B} C$

Solution :

$A B \overline{C} + A \overline{B} C + \overline{A} B C + A B C + A \overline{B} C$

$A B \overline{C} + A B C + A \overline{B} C + A \overline{B} C + \overline{A} B C$

$AB (\overline{C} + C) + A \overline{B} (\overline{C} + C) + A \overline{B} C$

$A B + A \overline{B} + \overline{A} B C$ (∴ $C + \overline{C} = 1$)

$A (B + \overline{B}) + \overline{A} B C$ (∴ $B + \overline{B} = 1$)

$A + \overline{A} B C$

$A + B C$ (∴ $A + \overline{A}B = A + B$)

De Morgan's Theorems

(i) De Morgan's First theorem

$\overline{A+B} = \overline{A} \cdot \overline{B}$

This theorem can be stated as follows: the complement of a sum equals the product of the complements.

Proof

$\overline{A+B} = \overline{A} \cdot \overline{B}$ can be proved by the giving all possible values for A and B and showing the L.H.S is equal to R.H.S.

(1) $A = 0, \quad B = 0$

Left : $\overline{A+B} = \overline{0+0} = \overline{0} = 1$

Right : $\overline{A} \cdot \overline{B} = \overline{0} \cdot \overline{0} = 1.1 = 1$

(2) $A = 0, \quad B = 1$

Left : $\overline{A+B} = \overline{0+1} = \overline{1} = 0$

Right : $\overline{A} \cdot \overline{B} = \overline{0} \cdot \overline{1} = 1.0 = 0$

(3) $A = 1, \quad B = 0$

Left : $\overline{A+B} = \overline{1+0} = \overline{1} = 0$

Right : $\overline{A} \cdot \overline{B} = \overline{1} \cdot \overline{0} = 0.1 = 0$

(4) $A = 1, \quad B = 1$

Left : $\overline{A+B} = \overline{1} + \overline{1} = \overline{1} = 0$

Right : $\overline{A} \cdot \overline{B} = \overline{1} \cdot \overline{1} = 0.0 = 0$

We cannot give any more values for A and B. Hence De Morgan's first theorem is proved. This proof can be represented in a truth table as shown below.

A	B	$Y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

A	B	$Y = \overline{A}.\overline{B}$
0	0	1
0	1	0
0	0	0
1	1	0

These table shows that $\overline{A+B}$ equal to $\overline{A.B}$ for each case. Therefore the expression are identical.

(ii) De Morgan's Second theorem

$\overline{A.B} = \overline{A} + \overline{B}$

This theorem can be stated as follows. The complement of a product equals the sum of the complements.

Proof

$\overline{A.B} = \overline{A} + \overline{B}$

(1) $A = 0, \quad B = 0$

Left : $\overline{A.B} = \overline{0.0} = \overline{0} = 1$

Right : $\overline{A} + \overline{B} = \overline{0} + \overline{0} = 1 + 1 = 1$

(2) $A = 0, \quad B = 1$

Left : $\overline{A.B} = \overline{0.1} = \overline{0} = 1$

Right : $\overline{A} + \overline{B} = \overline{0} + \overline{1} = 1 + 0 = 1$

(3) $A = 1, \quad B = 0$

Left : $\overline{A.B} = \overline{1.0} = \overline{0} = 1$

Right : $\overline{A} + \overline{B} = \overline{1} + \overline{0} = 0 + 1 = 1$

(4) $A = 1, \quad B = 1$

Left : $\overline{A.B} = \overline{1.1} = \overline{1} = 1$

Right : $\overline{A} + \overline{B} = \overline{1} + \overline{1} = 0 + 0 = 0$

We cannot give any more values for A and B. Hence De Morgan's second theorem is proved. This proof can be represented in a truth table as shown below.

A	B	$Y = \overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

A	B	$Y = \overline{A}+\overline{B}$
0	0	1
0	1	1
1	0	1
1	1	0

The table shows that $\overline{A.B}$ equal to $\overline{A} + \overline{B}$ for each case. Therefore the expression are identical.

Half and Full Adders

Half Adder

Block Diagram

Half Adder is shown in figure. As can be seen, it has two inputs B for applying the two binary digits to be added.

As is well known, binary addition of two bits always produces 2-bit output data i.e, one SUM and one CARRY. For example, (1+1) gives a sum of 0 and carry of 1. Also, (0+0) gives the sum 0 abd carry 0. That is why the adder has two outputs: one for SUM and the other for CARRY.

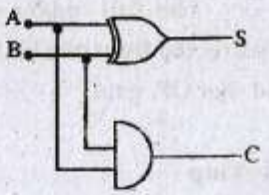
Input		Output	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

S - Sum
C - Carry

Truth Table lists the two columns of input, one of SUM and one of CARRY.

The SUM output has the same logic pattern as when A is XORed with B. Also, the CARRY output has the same logic pattern as when A is ANDed with B.

That is why a half-adder can be formed from a combination of one XOR gate and one AND gate as shown in figure.

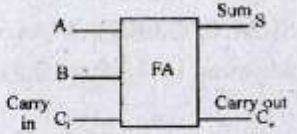


The circuit is called half-adder be-cause it cannot accept a carry in from previous additions. For that purpose we need a 3 - input adder called full adder.

Incidentally, the logical equation for the SUM and CARRY are $S = A \oplus B$ and $C = A.B$.

Full Adder

Full adder as shown in the block diagram of Fig 5.21 it has three inputs and two outputs. It can add 3 digits (or pits) at a time. The bits A and B which are to be added come from the two registers and the third input comes from the carry generated by the previous addition. It produces two outputs : SUM and CARRY - OUT.



The truth table gives all possible input/output relationships for the full adder.

A and B are the inputs from the respective digits of the registers to be added and C, is the input for any carry generated by the previous state.

The SUM output gives binary addition of A,B and C_i. The other output generate the carry C_o to be added to the next stage.

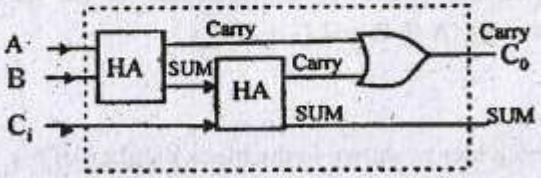
The full- adder can be constructed from two half-adder and one OR gate.

Input		Output		
A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$C_i = C_{in}$; $C_o = C_{out}$

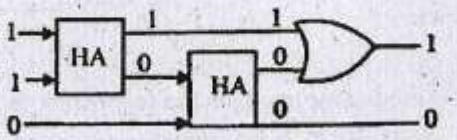
Working

Let us illustrate, with the help of two examples, how this full adder adds three bits..



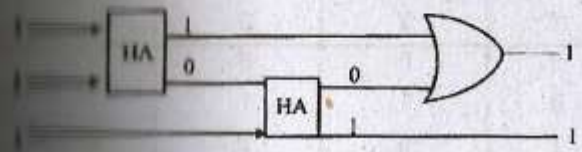
(i) A=1, B=1, C = 0

The full adder with these three inputs is shown in figure First half adder gives a sum of 0 and a carry of 1. The second HAgives a sum of 0 with a carry of 0. The final output is SUM 0, CARRY 1. As we know from the rules of binary addition, $1 + 1 + 0 = 10_2$ (i.e..decimal 2).



(ii) A = , B = 1, C = 1

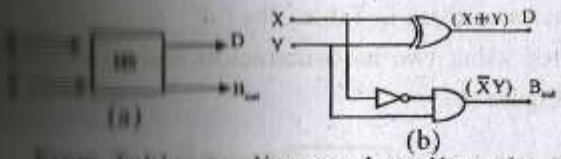
As detailed in Fig 5.25 we get a final SUM 1 with a CARRY 1. The result conforms to the binary addition : $(\quad)_2 = 11_2$ (i.e.,decimal).



HALF AND FULL SUBTRACTORS

(i) Half Subtractor

The half- subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, X (minuend) and Y (subtrahend) and two outputs D (difference) and B_{out} (borrow out). The logic symbol for a half- subtractor is shown in Figure(a). The truth table for half- subtractor is shown in Table. From the truth table, it is clear that the difference output is 0 if X = Y and 1 if X # Y; the borrow output B_{out} is 1 whenever X < Y. If X is less than Y subtraction is done by borrowing 1 from the next higher order bit.



From Table, as discussed earlier, the Boolean expression for difference (D) and Borrow out (B_{out}) can written as follows

From the above equations, the half - subtractor can be implemented using an Ex – OR gate, a NOT gate an AND gate as shown in Figure(b)

Half – Subtractor

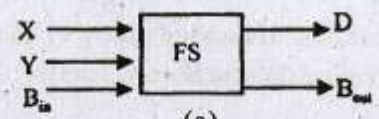
Truth table of half – subtractor

Inputs		Inputs	
Minuend X	Subtrahend Y	Difference D	Borrow B_{out}
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

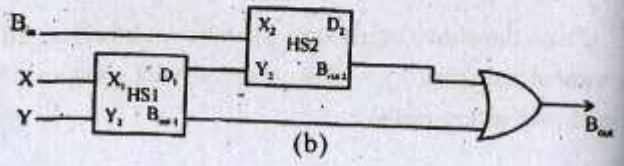
Full - Subtractor

A full- subtractor is a combinational circuit that performs subtraction involving three bits, namely minuend bit, subtrahend bit and the borrow from the previous stage. The logic symbol for full- subtractor is shown in Figure (a).

It has three inputs, X (minuend), Y (subtrahend) and Bin (borrow from previous stage), and two outputs D (difference) and B_{out} (borrow out). The truth table for the full-subtractor is given in Table. The full – subtractor Can be implemented using two half-subtractors and an OR gate as shown in Figure (b).



(a)



(b)

Full – Subtractor

Truth table of full – subtractor

Inputs		Inputs		
Minuend bit X	Subtrahend bit Y	Borrow B_{in}	Difference D	Borrow B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

From Table the sum of product expression for the difference (D) output can be written as:

$$D = \bar{X}\bar{Y}B_{in} + \bar{X}Y\bar{B}_{in} + X\bar{Y}\bar{B}_{in} + XYB_{in}$$

Simplifying the above expression

$$D = (\bar{X}\bar{Y} + XY)B_{in} + (\bar{X}Y + X\bar{Y})\bar{B}_{in}$$

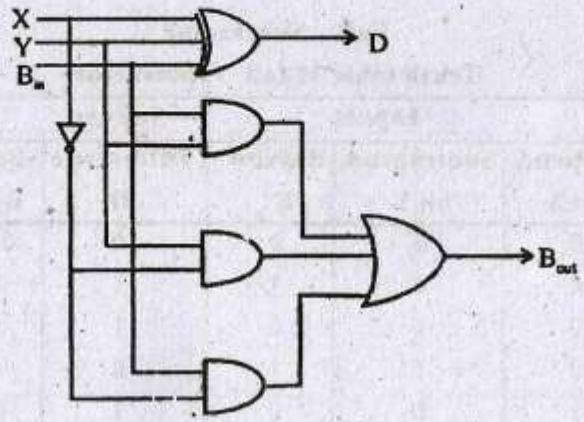
$$= (\overline{X \oplus Y})B_{in} + (X \oplus Y)\bar{B}_{in}$$

$$D = X \oplus Y \oplus B_{in}$$

Similarly, the sum of product expression for B_{out} can be written from the truth table as :

$$B_{out} = \bar{X}\bar{Y}B_{in} + \bar{X}Y\bar{B}_{in} + \bar{X}YB_{in} + XYB_{in}$$

The equation for B_{out} can be simplified using Karnaugh map is $B_{out} = \bar{X}Y + \bar{X}B_{in} + YB_{in}$



Once can notice that the equation for D is the same as the sum output for a full – adder, and the borrow output B_{out} resembles the carry output for full – adder except that one of the inputs is complemented. From these similarities, it is possible to convert a full- adder into a full-subtractor by merely complementing that input prior to its application to the input of gates which form the borrow output.

Decoders

A decoder is a combinational circuit that converts binary information from a input lines to a maximum of 2^n unique output lines. If the n-bit decoded information is not used or if there are don't care combinations, the decoder output will have less than 2^n outputs.

3-to-8 line decoder

The 3-to-8 line decoder circuit is shown in figure. The three inputs are decoded into eight outputs. Each output representing one of the minterms of the 3-input variables. The three inverters provide the complements of the inputs and each

one the eight AND gates generate one of the minterms. A particular application of this decoder would be a binary-to-octal conversion. The input variables may represent binary numbers and the outputs will then represent the eight digits in the octal number system. However, a 3-to-8 line decoder can be used for decoding any 3-bit code to provide eight outputs, one for each element of the code.

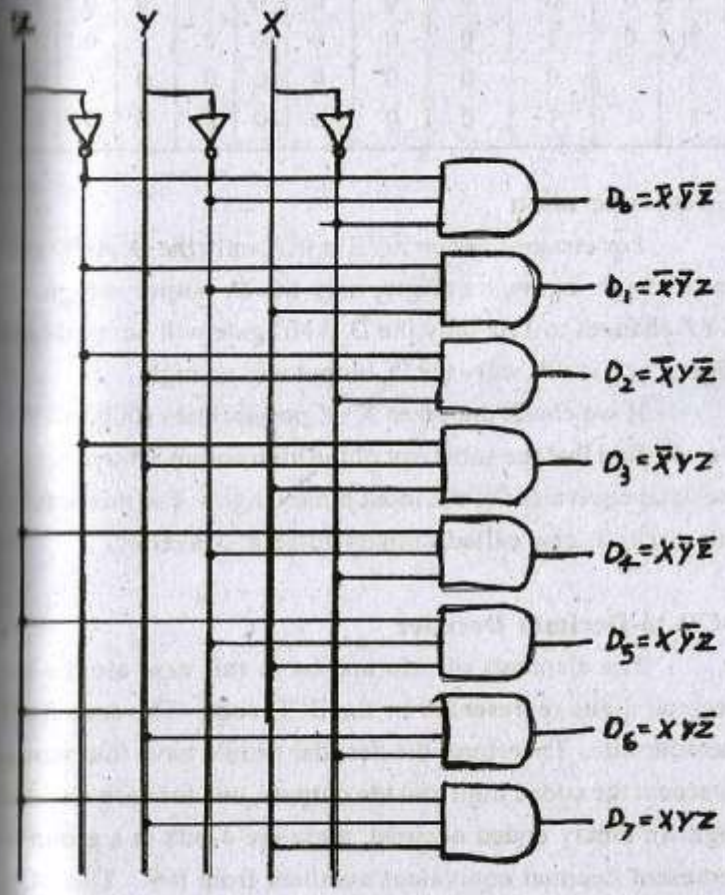


Table : Operation of the decoder input-output relationship

Inputs			Outputs							
X	Y	Z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Circuit operation

For instance, when XYZ is 011, only the D_3 AND gate has all high inputs, therefore, only the D_3 output is high. If XYZ changes to 110, only the D_6 AND gate will have all high inputs, as a result, only the D_6 output will go high.

If we check the other XYZ possibilities (000 to 111), we will find that the subscript of the high output always equals the octal equivalent of the input binary digits. For this reason, this circuit is also called a binary-to-octal converter.

BCD-to-Decimal Decoder

The elements of information in this case are the ten decimal digits represented by the BCD code. The code itself has four bits. Therefore, the decoder should have four inputs to accept the coded digit and ten outputs, one for each decimal digit. In binary coded decimal, there are 4-bits in a group to represent decimal equivalent numbers from 0-9. The BCD numbers corresponding to decimals 10 to 15 are not allowed and they can be considered as don't care terms. Let WXYZ

with Z as LSB and W as MSB be the number of BCD to be converted into decimal. The output for various combinations of W, X, Y and Z can be either 0, 1, 2, 3, 4, 5, 6, 7, 8 or 9 an each output will be a function of inputs W, X, Y and Z. The truth table for the BCD-to-decimal decoder is shown in table.

Since the circuit has ten outputs, the karnaugh maps are required to simplify each one of the output functions. There are six don't care conditions here and they must be taken into consideration when we simplify each of the output functions. Instead of drawing ten maps, we will draw only one map and write each of the output variables, D_0 to D_9, inside its corresponding minterm square as shown in figure. Six input combinations will never occur and they are marked as Xs.

W	X	Y	Z	Decimal
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	0	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	x
1	1	0	1	x
1	1	0	0	x
1	1	0	1	x
1	1	1	0	x
1	1	1	1	x

WX \ YZ	00	01	11	10
00	D_0	D_1	D_3	D_2
01	D_4	D_5	D_7	D_6
11	×	×	×	×
10	D_8	D_9	×	×

Map for simplifying a BCD-to-decimal decoder

It is the designer's responsibility to decide about the don't care conditions. Assume that it is decided to use them in such a way as to simplify the functions to the minimum number of literal. D_0 and D_1 cannot be combined with any don't care minterms. D_2 can be combined with the don't care minterm m_{10} to give : $D_2 = \overline{X}Y\overline{Z}$

The square with D_9 can be combined with three other don't care squares to give : $D_9 = WZ$.

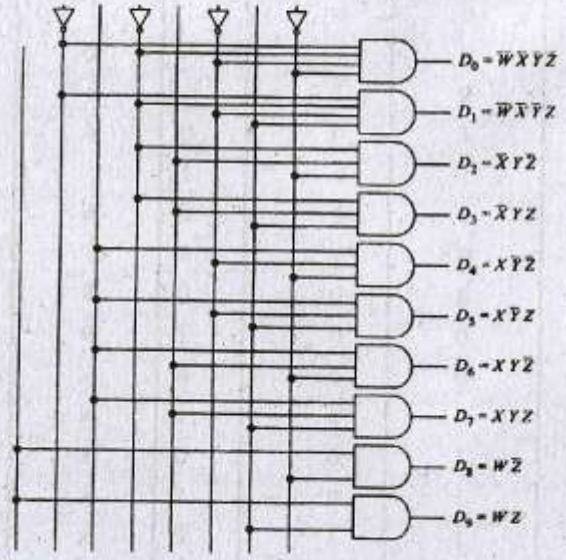


Figure : Logic circuit for BCD-to-decimal decoder

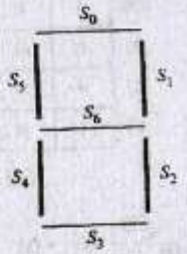
Using the don't care terms for the other outputs, we obtain the circuit shown in figure. Thus, the don't care terms cause a reduction in the number of inputs in most of the AND gates.

An analysis of the circuit in figure shown that the six invalid input combinations will produce outputs as shown in table.

Table : Partial truth table for the circuit of figure

Inputs				Outputs									
W	X	Y	Z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9
1	0	1	0	0	0	1	0	0	0	0	0	1	0
1	0	1	1	0	0	0	1	0	0	0	0	0	1
1	1	0	0	0	0	0	0	1	0	0	0	1	0
1	1	0	1	0	0	0	0	0	1	0	0	0	1
1	1	1	0	0	0	0	0	0	0	1	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1	0	1

Most digital systems such as BCD computers and calculators use BCD numbers which are converted into seven-segment codes with the help of a combinational logic circuit. The seven segments S_0, S_1, S_2, S_3, S_4, S_5, S_6 and S_7 are shown in figure.



AB \ CD	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	×	×	×	×
10	1	1	×	×

$S_0 = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + B\,\overline{C}\,\overline{D}$

(a) To find S_0

AB \ CD	00	01	11	10
00	1	1	1	1
01	1	0	1	0
11	×	×	×	×
10	1	1	×	×

$S_1 = B\overline{C}D + BC\overline{D}$

(b) To find S_1

01	1	1	1	1
11	×	×	×	×
10	1	1	×	×

$S_2 = \overline{B}C\overline{D}$

(c) To find S_2

AB \ CD	00	01	11	10
00	1	0	1	1
01	0	1	0	1
11	×	×	×	×
10	1	1	×	×

$S_3 = \overline{A}\,\overline{B}\,\overline{C}D + B\overline{C}\,\overline{D} + BCD$

(d) To find S_3

AB \ CD	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	×	×	×	×
10	1	0	×	×

$S_4 = D + B\overline{C}$

(e) To find S_4

AB \ CD	00	01	11	10
00	1	0	0	0
01	1	1	0	1
11	×	×	×	×
10	1	1	×	×

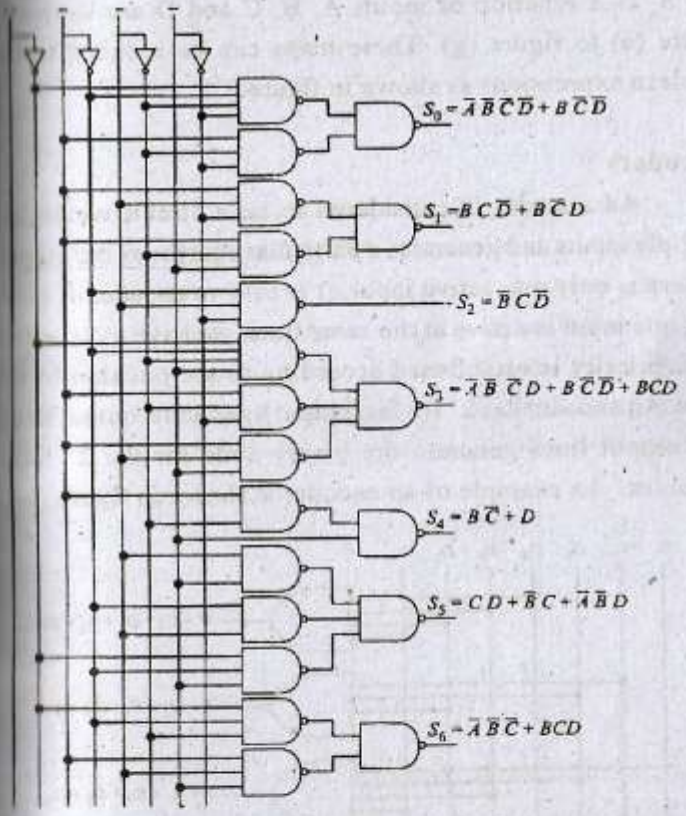
$S_5 = CD + \overline{B}C + \overline{A}\,\overline{B}D$

(f) To find S_5

AB \ CD	00	01	11	10
00	0	0	1	1
01	1	1	0	1
11	×	×	×	×
10	0	1	×	×

$S_6 = \overline{A}\,\overline{B}\,\overline{C} + BCD$

(g) To find S_6



The truth table for BCD-to-seven segments is shown in table.

As the numbers which are greater than 9 are the not permitted combinators, it is assumed that they will not occur. This truth table can be constructed by knowing for a particular decimal number between 0 to 9, which of the seven segments will be lighted and which will not be lighted. For example, for displaying 6, all segments will be lighted except S_1. The Karnaugh maps for these seven segments S_0, S_1, S_2, S_3, S_4, S_5 and S_6 as a function of inputs A, B, C and D are shown in figure (a) to figure (g). These maps can be reduced to the Boolean expressions as shown in figure.

Encoders

An encoder is considered to be a circuit which has multiple inputs and generates a particular address as the output. If there is only one active input, it is easy to encode. If more than one input is active at the same time, we have to establish some priority is established according to the position of the input. An encoder has 2" (or less) input lines and n output lines. The output lines generate the binary code for the 2" input variables. An example of an encoder is shown in figure.

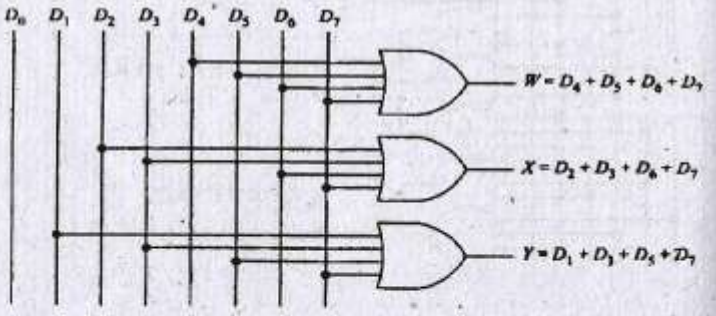


Figure : Eight – input priority encoder (or an octal-to-binary encoder)

Table : Truth table of octal-to-binary encoder.

Inputs			Outputs							
X	Y	Z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

The low order output bit is a 1 if the input octal digits are 4, 5, 6 or 7. The output X is a 1 for octal digits 2, 3, 6 or 7. Here D_0 is not connected to any OR gate. The binary outputs must be all 0s in this case. An all 0s output is also obtained when all inputs are all 0s. This discrepancy can be resolved by providing one more output to indicate the fact that all inputs are not 0s.

The reduced or minimal expression for W, X and Y, as obtained form table or Karnaugh map, can be expressed as follows :

$$W = D_4 + D_5 + D_6 + D_7$$
$$X = D_2 + D_3 + D_6 + D_7$$
$$X = D_1 + D_3 + D_5 + D_7$$

The realization of the above Boolean expression is shown in figure. In this circuit when D_0 is 1, the outputs W, X and Y are all 0s and we also have all the outputs as 0 when all inputs are 0s. To take care of this drawback, we can add one more output line which will be 1 when all the inputs are 0s. Also, we can take care of the priority.

The encoder in figure assumes that only one input line can be equal to 1 at any time; otherwise the circuit has no meaning. This circuit has eight inputs and could have $2^8 = 256$ possible input combinations. Only eight of these combinations have any meaning. The other input combinations are don't care conditions.

Gray – to – Binary Encoder

To design a circuit for converting Gray code to Binary code we proceed as follows : Karnaugh map each on i.e, we draw four Karnaugh map corresponding B_1, B_2, B_3 and B_4.

Table Truth table for converting Gray code to binary digit

Decimal	Gray				Binary			
	G_1	G_2	G_3	G_4	B_1	B_2	B_3	B_4
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	1	0	0	1	0
3	0	0	1	0	0	0	1	1
4	0	1	1	0	0	1	0	0
5	0	1	1	1	0	1	0	1
6	0	1	0	1	0	1	1	0
7	0	1	0	0	0	1	1	1
8	1	1	0	0	1	0	0	0
9	1	1	0	1	1	0	0	1
10	1	1	1	1	1	0	1	0
11	1	1	1	0	1	0	1	1
12	1	0	1	0	1	1	0	0
13	1	0	1	1	1	1	0	1
14	1	0	0	1	1	1	1	0
15	1	0	0	0	1	1	1	1

The outputs B_1, B_2, B_3 and B_4 can be expressed in minterms as follows :

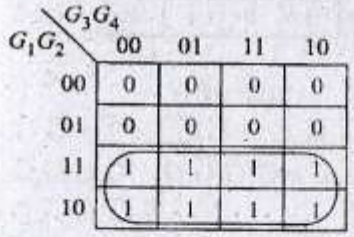
$B_1 = \Sigma m\,(8, 9, 10, 11, 12, 13, 14, 15)$

$B_2 = \Sigma m\,(4, 5, 6, 7, 8, 9, 10, 11)$

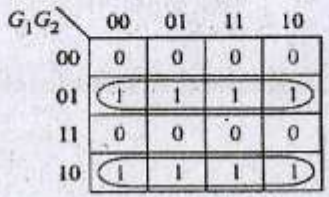
$B_3 = \Sigma m\,(2, 3, 4, 5, 6, 8, 9, 14, 15)$

$B_4 = \Sigma m\,(1, 2, 4, 7, 8, 11, 13, 14)$

The Karnaugh maps of these variables are shown in figure.

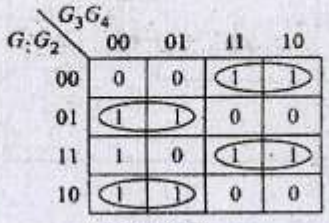


Map of B_1



Map of B_2

$B_2 = \bar{G}_1 G_2 + G_1 \bar{G}_2 = G_1 \oplus G_2$



Map of B_3

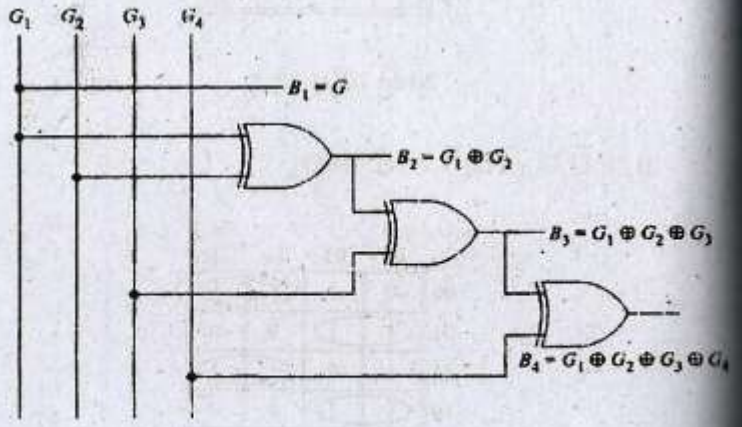
$$B_3 = \overline{G}_1\overline{G}_2G_3 + \overline{G}_1G_2\overline{G}_3 + G_1G_2G_3 + G_1\overline{G}_2\overline{G}_3$$
$$= G_3(G_1 \oplus G_2) + G_3(G_1 \oplus G_2)$$
$$= G_1 \oplus G_2 \oplus G_3$$

G_1G_2 \ G_3G_4	00	01	11	10
00	0	1	0	1
01	1	0	1	1
11	0	1	0	1
10	1	0	1	0

Map of B_4

$$B_4 = \overline{G}_1\overline{G}_2\overline{G}_3G_4 + \overline{G}_1\overline{G}_2G_3\overline{G}_4 + \overline{G}_1G_2\overline{G}_3\overline{G}_4 + \overline{G}_1$$
$$= G_2G_3G_4 + G_1G_2\overline{G}_3G_4 + G_1G_2G_3\overline{G}_4$$
$$+ G_1\overline{G}_2\overline{G}_3\overline{G}_4 + G_1\overline{G}_2G_3G_4$$
$$= \overline{G}_1\overline{G}_2(G_3 \oplus G_4) + \overline{G}_1G_2\overline{(G_3 \oplus G_4)}$$
$$+ G_1G_2(G_3 \oplus G_4) + G_1G_2\overline{(G_3 \oplus G_4)}$$

The circuit realization using exclusive OR gates is shown in Fig.



BCD – to – Excess – 3 and Excess – 3 – to – BCD Encoder

To design a circuit for converting BCD – to – excess – 3 code and also for converting Excess – 3 – to – BCD we proceed as follows :

The conversion table for BCD – to – Excess – 3 code is shown in table.

Table - Truth table for converting BCD – to – Excess – 3 code

Decimal Number	BCD code				Excess – 3 code			
	B_1	B_2	B_3	B_4	E_1	E_2	E_3	E_4
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	00	0	1	1	1	0	0
10 to 15	Don't care terms							

B_1B_2 \ B_3B_4	00	01	11	10
00	0	0	0	0
01	0	1	1	1
11	×	×	×	×
10	1	1	×	×

$E_1 = B_1 + B_2B_4 + B_2B_3$

Map for E_1

B_1B_2 \ B_3B_4	00	01	11	10
00	0	1	1	1
01	1	0	0	0
11	×	×	×	×
10	0	1	×	×

$E_2 = B_2\bar{B}_3\bar{B}_4 + \bar{B}_2B_4 + \bar{B}_2B_3$

Map for E_2

B_1B_2 \ B_3B_4	00	01	11	10
00	1	0	1	0
01	1	0	1	0
11	×	×	×	×
10	1	0	×	×

$E_3 = \bar{B}_3\bar{B}_4 + B_3B_4 + B_3 \oplus B_4$

Map for E_3

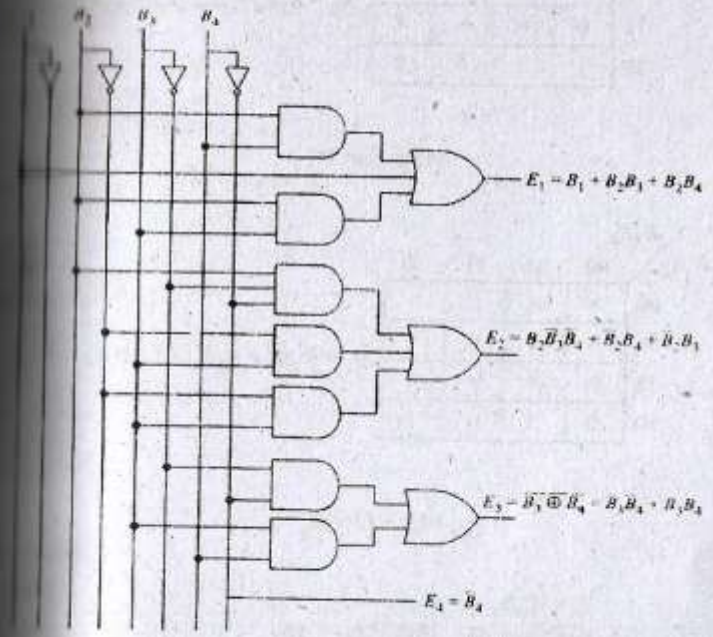
B_1B_2 \ B_3B_4	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	×	×	×	×
10	1	0	×	×

$E_4 = \bar{B}_4$

Map for E_4

To convert Excess – 3 code into BCD, we consider the truth table for BCD – to – Excess conversion and treat E_1, E_2, E_3 and E_4 as input and the outputs are considered to be B_1, B_2, B_3 and B_4. As the terms corresponding to decimal numbers 0, 1, 2, 13, 14, 15 will not appear in Excess – 3 code, these terms are considered don't care terms. The Boolean expression

obtained from the Karnaugh maps for B_1, B_2, B_3 and B_4 are shown in figure



Logic circuit

E_1E_2 \ E_3E_4	00	01	11	10
00	×	×	0	×
01	0	0	0	0
11	1	×	×	×
10	0	0	1	0

$B_1 = E_1E_2 + E_1E_2E_3$

Map for B_1

00	×	×	0	×
01	0	0	1	0
11	0	×	×	×
10	1	1	0	1

$B_2 = \bar{E}_2\bar{E}_4 + E_2E_3E_4 + E_1\bar{E}_3E_4$

Map for B_2

E_1E_2 \ E_3E_4	00	01	11	10
00	×	×	0	×
01	0	1	0	1
11	0	×	×	×
10	0	1	0	1

$B_3 = \bar{E}_3E_4 + E_3\bar{E}_4 = E_3 \oplus E_4$

Map for B_3

E_1E_2 \ E_3E_4	00	01	11	10
00	×	×	0	×
01	1	0	0	1
11	1	×	×	×
10	1	0	0	1

$B_4 = \bar{E}_4$

Map for B_4

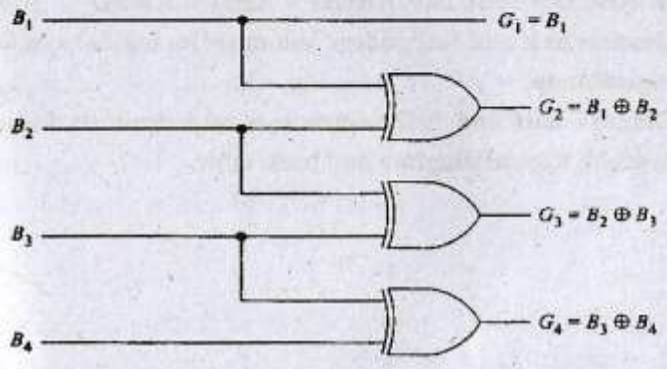
The realization of above expressions is shown in figure

Decoder for Binary – to – Gray code

The covert a binary – to – Gray code, the significant bit is noted. This MSB is added to the bit in the next position

The sum is recorded and carry if any generated is neglected. This procedure is repeated till the last bit of the binary number is noted.

The conversion table of binary – to – Gray code is shown in figure.



Two Mark Questions

1. Write Boolean's laws of Associative and distributive?
2. State De Morgan's theorems?

Four Mark Questions

1. Explain the half adder with the help of truth table?
2. Explain the full adder with the help of truth table?
3. Write a note on half subtractor.
4. Write a note on full subtractor.
5. Prove that following

   i. AB + AB = A

   ii. A + AB = A + B

   iii. (A+B) (A+B) = A